Static Reliability of Bridged-Grain Poly-Si TFTs

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Abstract

The characteristics of bridged-grain (BG) poly-Si thin film transistors (TFTs) with different BG periods and the static reliability of BG poly-Si TFTs was examined and discussed. The characterizations show that the length of the sub-channels mainly affects the on-state current and the sub-threshold characteristics. BG TFTs exhibit better hot carrier reliability, better self-heating reliability, better negative bias temperature instability and good immunity against water.

Keywords: *Bridged grain, polycrystalline silicon, thin film transistors, static reliability, doping*

1. Introduction

To achieve high-resolution display and system-on-panel (SOP) application, high-performance thin film transistors (TFTs) with good reliability are thus required [1]. Poly-Si TFTs, which have larger mobility [2] and are more stable [3, 4] than metal oxide TFTs, have been actively investigated. The most widely adopted poly-Si technology is laser annealing method. Excimer laser annealing (ELA) [5] and sequential lateral solidification (SLS) [6] technology could produce poly-Si with fewer defects. However, at the same time the as-generated poly-Si film also suffers from material non-uniformity due to the random distribution of grain boundaries (GBs) [7]. Non-uniformity, which will directly result in non-uniform light emission over the whole panel, is highly undesirable for displays. Solid phase crystallization (SPC) [8] and metal induced crystallization (MIC) [9] are alternative ways to obtain poly-Si film with small grain size and better uniformity. Nevertheless, the performance of TFT based on SPC/MIC film is still not satisfactory for advanced display applications. Several nano/micro-structures [10-12], such as trenched body [10] and 3-D finlike channels [11, 12] are proposed to improve device performance. However, to get these nano/micro-structures requires fine patterning of SiO_2 or poly-Si layers, which is incompatible to the conventional process in industry. Moreover, neither method could significantly improve the on- and off-state characteristics at the same time. Additionally, such nano/micro-structures may also bring reliability issues.

Bridged-grain (BG) technology [13] has been introduced to improve the on/off-current ratio, threshold voltage (V_{th}), sub-threshold swing (SS) and gate induced drain leakage (GIDL) [14]. These improvements are attributed to the application of submicrometer-scale BG structures to introduce short channel effects (SCEs), provide shortcuts to improve the current flow and reduce the drain lateral electric field (E_x) by multi-gate effect.

In this work, dependence of electrical properties of BG TFTs on the number and width of the intra-channel doped regions are studied. The characterization results show that the length of the sub-channels mainly affects the on-state current and the sub-threshold characteristic. Reliability of BG TFTs under various DC bias stresses is then performed. BG TFTs are more reliable under hot carrier (HC) stress, self-heating (SH) stress, negative bias temperature (NBT) stress and thermal-humidity (T-H) stress.

2. Experimental

Schematic illustration of device fabrication process flow is shown in Figure 1. Four-inch sized silicon wafers covered with 500 nm thermal oxide were applied as the starting substrates and a layer of amorphous silicon (a-Si) was deposited onto the substrate through low pressure chemical vapor deposition (LPCVD). SPC [13] or MIC [15] method was employed to convert a-Si film into poly-Si film. After crystallization, photoresist was spin coated and patterned into gratings with different periods (Λ) and aspect ratios. Structures of the patterned photoresist were captured by the scanning electron microscope (SEM) as shown in Figure 2. Boron ions were then implanted into the exposed areas through the grating with energy of 23keV and a dose of $2\times10^{15}/cm^2$. After implantation, the photoresist was removed and the poly-Si layer was then patterned into active islands, followed by a layer of SiO_2 deposition through LPCVD at 425ºC as gate dielectric. Then 300nm aluminum was sputtered and patterned as gate electrodes and the source\drain were formed through a self-aligned 33keV boron implantation at a dosage of $4\times10^{15}/cm^2$. The contact holes were defined through another 500 nm SiO_2 layer which was adopted as an isolation layer. A layer of 700nm Al-1%Si was sputtered and patterned as testing pads. The devices were then sintered in forming gas for 30 min at 420ºC. No further passivation was applied to these devices.

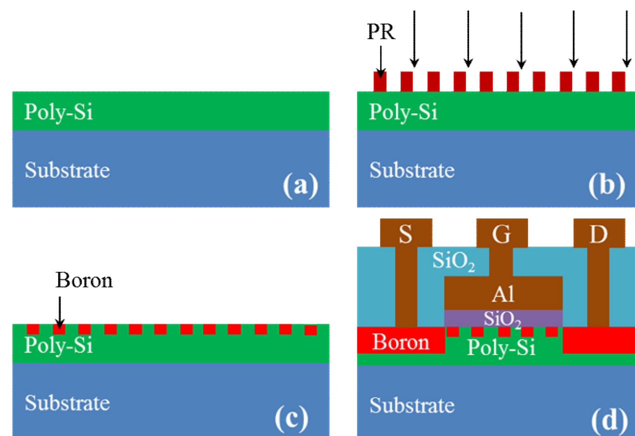

Figure 1. Schematic illustration of device fabrication process flow. (a) Poly-Si on the substrate. (b) BG pattern formation by patterning photoresist. (c) Active channel with BG line doping. (d) Cross-section of BG TFT.

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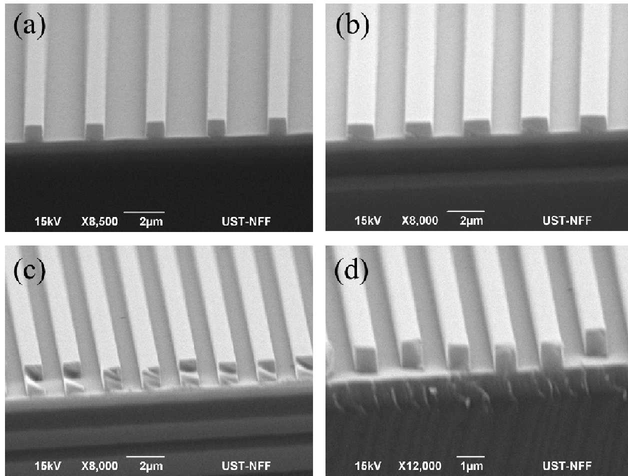

Figure 2. SEM images of the patterned photoresist gratings. (a) Λ=3μm, 2μm exposed. (b) Λ=3μm, 1.5μm exposed. (c) Λ=2μm, 1μm exposed. (d) Λ=1.6μm, 0.8μm exposed.

Table 1. Device labels and respective configurations

BG configuration as in Fig.2	*L* on the layout (μm)	L_{eff} (μm)	No. of BG regions	Sample label
(a)	18	6	6	A1
(b)	18	9	6	B1
(c)	12	6	6	C1
(c)	18	9	9	C2
(d)	18	9	11	D1
No BG	18	18	N.A.	E1

To characterize the effect of the number and width of the intra-channel doped regions more efficiently, TFTs with different BG configurations were labeled and summarized in Table 1. The channel width (W) is fixed at 12 μm and the channel length (L) on the layout varies from 4 to 20μm. For static reliability test, the Λ equals to 1μm and 0.5μm is exposed. Four groups of stresses were applied, namely DC HC stress (stress V_d=−40V, stress V_g=−15V), DC SH stress (stress power density p=75.8μW/μm^2), DC NBT stress (V_g–V_{th}=−25V) and T-H stress. The T-H treatment to the wafer was performed in the air with 95% relative humidity at 80°C for 50 hours. Device degradation was characterized by variation rate of on-current (I_{on}).

3. Results and Discussion

Effect of the Number and Width of the Intra-Channel Doped Regions

TFT A1, B1, C2, D1 and E1 have the same device dimensions on the layout. The comparison of their transfer characteristics is shown in Figure 3. From Figure 3, it can be seen that the effect of the BG can be observed for all TFTs with BG configurations shown in Fig.2. The on-state characteristics can be more clearly observed in the curves plotted in linear scale. It can be observed that sample A1 exhibits the largest on-state current. This is obviously due to the shorter L_{eff} of A1 (L_{eff}=6μm) than the other BG devices (L_{eff}=9μm). For B1, C2 and D1, the on-state current follows the relationship: D1>C2>B1. This suggests that devices with a shorter BG period give larger on-state current, which is the result of stronger SCEs and grain size effect [13]. The effect of L_{eff} can be observed from the comparison between A1 and B1. The L, the Λ of the grating and the number of BG lines within the channel are the same for A1 and B1. As observed from Figure 3, A1 produces much larger I_{on} due to shorter L_{eff}. Additionally, the leakage current of A1 and B1 are comparable, which will be discussed below. A comparison between A1 and C1 is also given as shown in Figure 4. A1 and C1 have the same L_{eff}, the same number of BG regions in the channel and the same L for every sub-channel. Therefore, the characteristics of A1 and C1 are almost the same.

To study the relationship between the off-state current and the number of BG regions, the off-current (I_{off}) of the TFTs with different L (4μm~20μm) was measured. The number of BG regions for the TFTs with different BG configurations (as shown in Figure 2) is listed in Table 2. The measurement results are shown in Figure 5. It can be seen that the effect of the leakage suppression saturated at a large number of BG lines. For TFTs with a larger sub-channel length, 5 ~ 6 BG lines are already very effective in suppressing the leakage current. However, with larg-

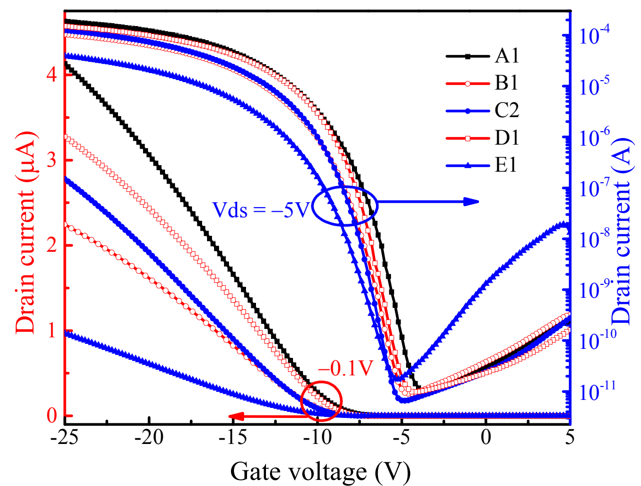

Figure 3. Comparison of the transfer characteristics of the TFTs with same *L* on the layout.

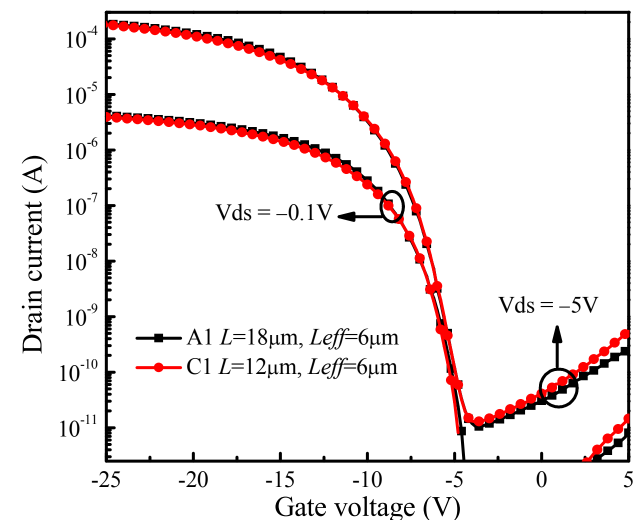

Figure 4. Comparison of the transfer characteristics of A1 and C1.

Table 2. Number of BG regions in MIC poly-Si TFTs with different L and BG configurations

L \ NO. (BG as in Fig.2)	(b)	(c)	(d)
4 μm	1	2	2
6 μm	2	3	3
8 μm		4	5
10 μm	3	5	6
12 μm	4	6	7
14 μm		7	8
16 μm	5	8	10
18 μm	6	9	11
20 μm		10	12

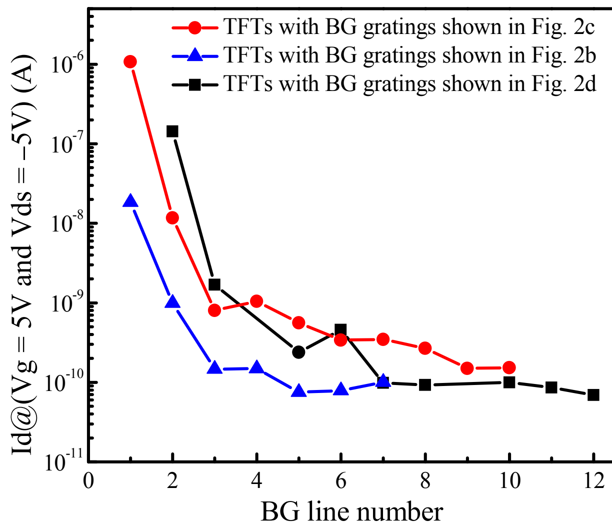

Figure 5. Dependence of off-state leakage on number of BG lines.

-er sub-channel length the contribution of the SCEs to the on-state current is also reduced.

Static Reliability

Shown in Figure 6 is I_{on} degradation of normal MIC TFTs and BG MIC TFTs under HC stress, SH stress and NBT stress. The W of stressed TFTs is fixed at 10μm and the effective channel length (L_{eff}) is fixed at 6μm. For the same HC stress, as represented by black lines in Figure 6, BG TFT exhibits much more reliable HC characteristic. Such improved HC reliability in BG TFTs is mainly attributed to E_x reduction by BG lines at drain side. For the SH stress, at the same stress power density (red lines in Figure 6), BG TFT also exhibits better SH reliability than normal TFT. High power generated by high voltage stresses could break/distort some of strong Si-Si bonds located at GBs in the whole channel [16], decreasing I_{on}. For the improved SH in BG TFTs, it may be due to GBs screened by heavily doped BG lines in the channel. For the NBT stress, BG TFT again shows better NBT reliability (blue lines).

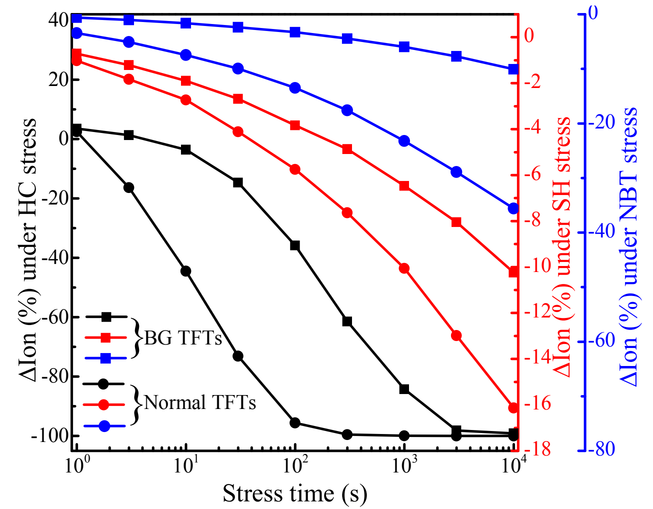

Figure 6. I_{on} degradation of normal MIC TFTs and BG MIC TFTs under HC stress, SH stress and NBT stress.

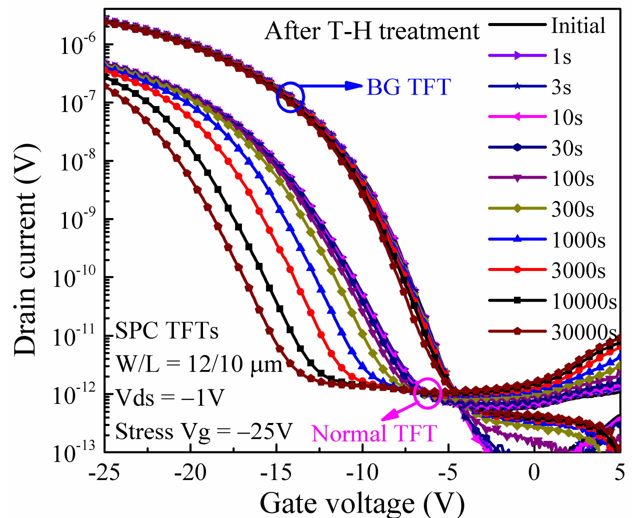

Figure 7. After T-H treatment, transfer curve degradation comparison between normal SPC TFT and BG SPC TFT under the same V_g stress.

Moisture stress test is also performed using T-H treatment. As shown in Figure 7 is transfer curve degradation comparison between normal SPC TFT and BG SPC TFT under the same V_g stress after T-H treatment. Obviously, after the same T-H treatment, TFT exhibits much more reliable characteristic. It is known that water diffusing into gate oxide could enhance NBTI degradation by providing additional OH^- [17]. Therefore, after T-H treatment, NBT degradation of normal TFT is much larger than the one without T-H treatment under the same NBTI stress (not shown here). However, for BG TFTs, water seems to have no influence on NBTI degradation by comparison between with and without T-H treatment (not shown here), indicating BG TFTs have higher immunity against the water.

4. Conclusion

In this work, characteristics of BG TFTs with larger BG periods are studied. It is shown that the length of the sub-channels mainly affects the on-state current and the sub-threshold

characteristics. Shorter sub-channels result in stronger SCEs and a larger I_{on}. The leakage current is mainly affected by the number of BG regions inside the channel, and can be well controlled with 5-6 BG lines for BG TFTs with sub-channel lengths of 1μm or above. For shorter sub-channels, a larger number of BG regions are necessary to effectively suppress the leakage current. For static reliability of BG TFTs, different combinations of V_d stress and V_g stress is investigated. The test results reveal that BG TFTs exhibit better HC reliability, better SH reliability, better NBTI reliability and good immunity against the water.

5. Acknowledgement

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6. References

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