Moisture Related Instability in p-Type Low Temperature Polycrystalline Silicon Thin Film transistors

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ABSTRACT

The unreliable behaviors of low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) after a period of storage are confirmed to be related to the moisture by the observation of enhanced negative bias temperature instability (NBTI) after humidity treatments and the observation of decreased NBTI degradation after hard bake treatment. PECVD passivation layers of combined SiO_2 and Si_3N_4 deposited on the top of low temperature LTPS TFT structure can effectively prevent the moisture from penetrating into the TFT structure and improve the device reliability.

Keywords: low temperature polycrystalline silicon, thin film transistors, moisture related instability, passivation layer.

INTRODUCTION

Low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have become very promising devices to achieve the integration of peripheral circuit and active matrix [1]. The reliability of LTPS TFTs is of vital importance for TFT based applications. In this work, moisture related instability in p-type LTPS TFTs is investigated. It is found that LTPS TFTs after a period of normal storage become unreliable and it is confirmed that this unreliable behavior is caused by the moisture through the observation of enhanced negative bias temperature instability (NBTI) with humidity treatments and the observation of decreased NBTI with hard bake. To solve this moisture related instability problem, passivation layers of combined SiO_2 and Si_3N_4 are deposited on the top of poly-Si TFT structure using PECVD technique and the stress test results reveal that TFTs with passivation layers can effectively prevent the moisture from penetrating into the TFT structure and improve device reliability.

EXPERIMENT

There are three kinds of p-type LTPS TFTs used in this study, solid phase crystalline (SPC) TFTs, excimer laser annealed (ELA) TFTs and metal induced lateral crystallization (MILC) TFTs. The maximum process temperature is 600ºC. All devices are in conventional self-aligned top-gate structure. Detailed process flow can be found elsewhere [2].

TFTs under test are 12 μm in width (*W*) and 10 μm in channel length (*L*). Typical NBTI stress (stress V_g= –25V and grounded source/drain) is applied to test the device reliability. Devices are measured before and after stress by using Agilent 4156B semiconductor parameter analyzer. The wafer humidity treatment is performed in the 90% relative humidity air at 80ºC for 50 hours and the wafer hard bake is carried out on a hot-plate at 150ºC for 15 hours. Passivation layers are deposited using PECVD.

RESULTS AND DISCUSSIONS

Shown in Fig.1a are transfer curve measurements of a fresh SPC TFT (dash lines) and a SPC TFT after 15 day normal storage (solid lines). For an fresh SPC TFT, the transfer curves for the three times measurements overlap each other well. However, after 15 day normal storage, the on-current (I_{on}) decreases (solid lines) compared to the fresh SPC TFT and for each measurement all the transfer curves no longer overlap. Storage induced instability occurs. Similar degradation phenomena are also observed in ELA TFTs and MILC TFTs as shown in Fig.1b and Fig.1c respectively. During the storage, besides the intrinsic change, the moisture in the air may diffuse into the TFT structure and cause the reliability problems. Additionally, by comparing different kinds of TFTs shown in Fig.1, MILC TFTs exhibit more reliable performance than others.

To verify whether the instability of LTPS TFTs after a period of storage is related to the moisture in the air, a series of experiments are designed. First, a typical NBTI stress is applied to an MILC TFT without any additional operation. Shown in Fig.2a is the time evolution of transfer characteristic of an MILC TFT under stress V_g= –25V. Typ-

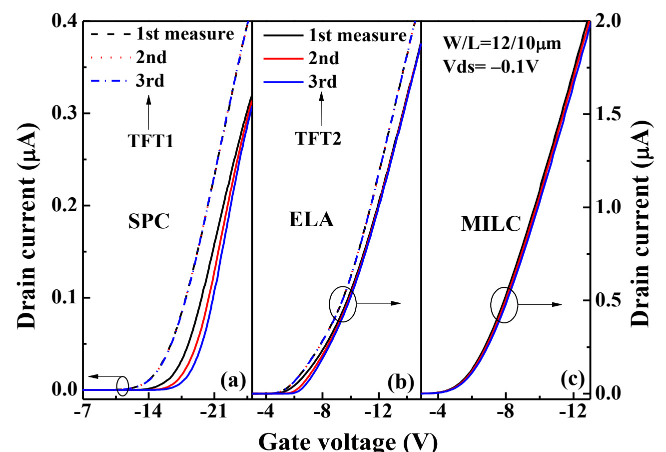

Fig.1: (a) Transfer curve measurements of a fresh SPC TFT (dash lines) and a SPC TFT after 15 days storage (solid lines). (b) Transfer curve measurements of a fresh ELA TFT (dash lines) and an ELA TFT after 17 days storage (solid lines). (c) Transfer curve measurements of a fresh MILC TFT (dash lines) and a MILC TFT after 15 days storage (solid lines).

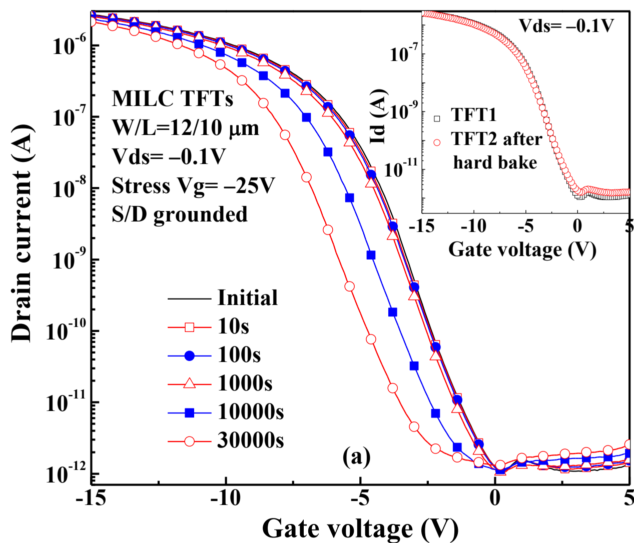

Fig.2: (a) Before hard bake, time evolution of transfer characteristic under typical NBTI stress for MILC TFTs, measured at V_{ds}= –0.1V. The inset is the transfer curve of TFTs measured before and after hard bake treatment.

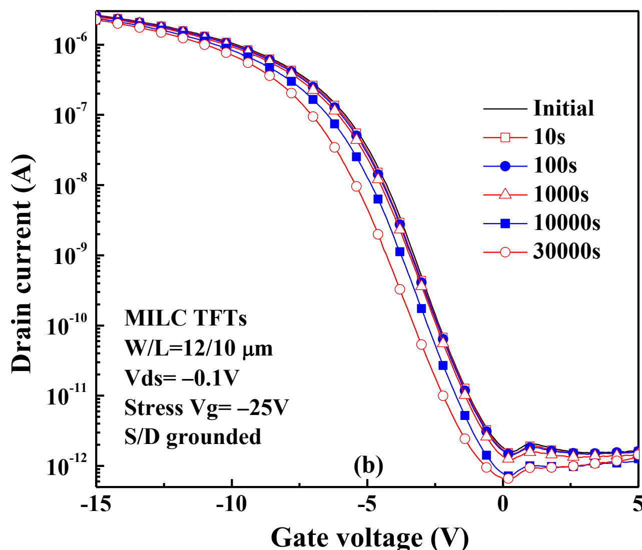

Fig.2: (b) After hard bake, time evolution of transfer characteristic under typical NBTI stress for MILC TFTs, measured at V_{ds}= –0.1V.

-ical NBTI degradation behaviors, a negative shift of threshold voltage (V_{th}), almost no change in sub-threshold region and degradation slope of ~0.30 (Fig.3), are observed due to the interface and/or grain boundary trap generation [3-4]. After the NBTI stress test, the wafer is hard baked. After the hard bake, the same NBTI stress is applied to another MILC TFT with the same *W/L* when the wafer cools down to room temperature. Shown in Fig.2b is the transfer curve degradation of the MILC TFT under NBTI stress after the hard bake treatment. It is found that both I_{on} degradation and V_{th} negative shift of hard baked TFT are improved compared to that of the TFT without hard bake treatment, also as shown in Fig.3. It is considered that the improved reliability due to the hard bake may arise from some repaired defects during hard bake or moisture in the TFT structure released by high temperature since the H_2O near the interface could increase the concentration of SiOH group which could enhance the NBTI degradation [5-6]. H-

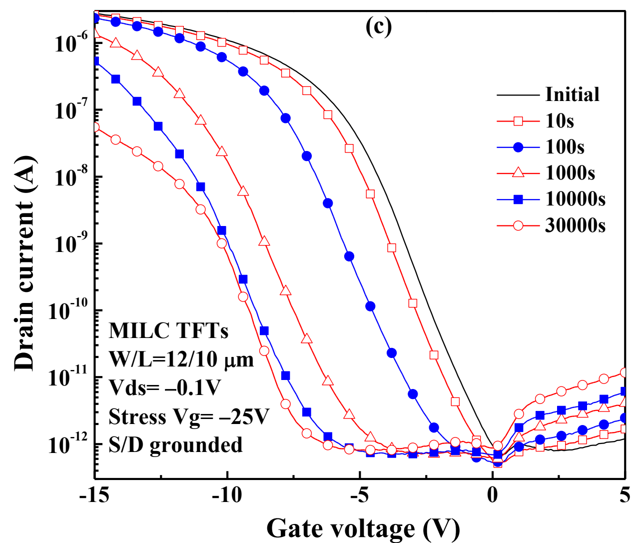

Fig.2: (c) After humidity treatment, time evolution of transfer characteristic under typical NBTI stress for MILC TFTs, measured at V_{ds}= –0.1V.

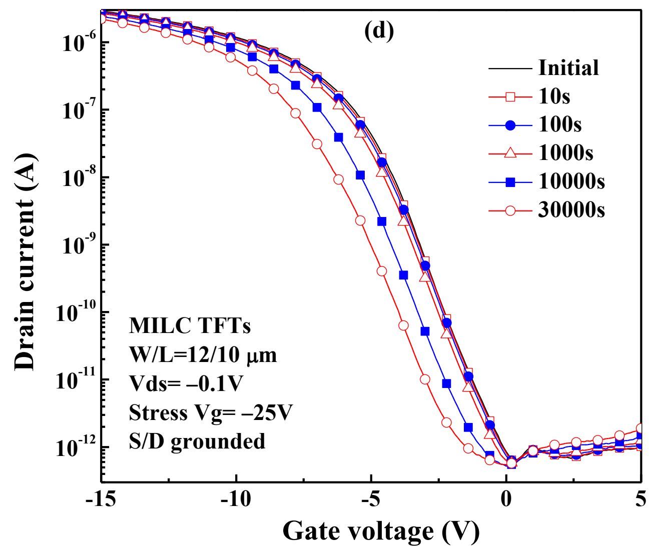

Fig.2: (d) After 15 hours hard bake, time evolution of transfer characteristic under typical NBTI stress for MILC TFTs, measured at V_{ds}= –0.1V.

-owever, according to the report [7], 150ºC hard bake could hardly repair the defects in LTPS TFTs, which can also be verified by the observation shown in the inset of Fig.2a. Transfer curves of TFTs overlap each other well before and after hard bake treatment. Based on the above discussion, it is believed that the improved reliability by the hard bake is mainly due to the evaporation of moisture existing in the TFT structure.

To further confirm the above statement, a humidity treatment is applied to the wafer. After the humidity treatment, another TFT is stressed under the same NBTI bias when the wafer cools down to room temperature. Greatly enhanced NBTI degradation is observed as shown in Fig.2c and Fig.3. Both I_{on} and V_{th} degenerates dramatically. The ability and quantity of H_2O diffusing into TFT structure is greatly enhanced by humidity treatment and therefore the NBTI degradation is increased as discussed before [5-6]. After the stress test, the wafer is the-

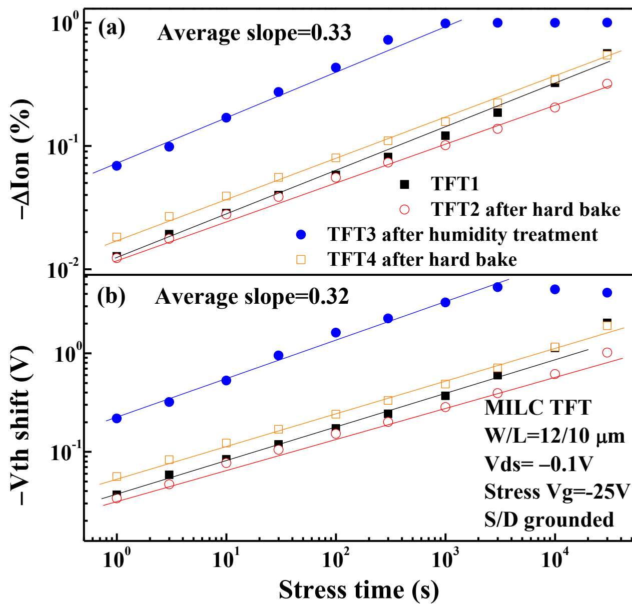

Fig.3: After different treatments, dependence of (a) I_{on} degradation and (b) V_{th} shift on stress time for MILC TFTs under the same typical NBTI stress.

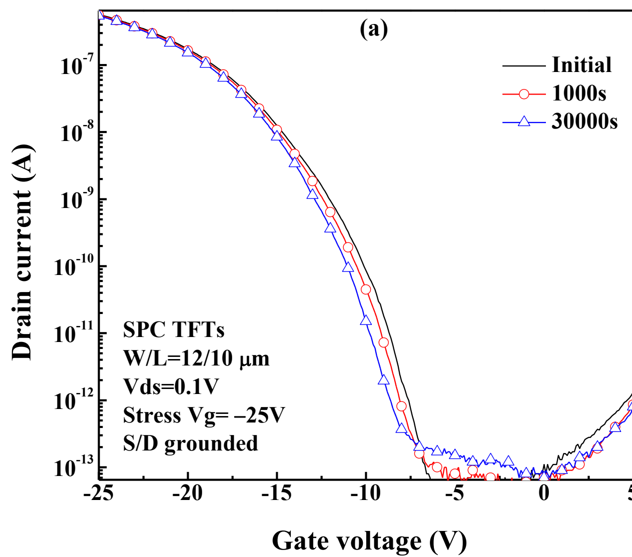

Fig.4 (a) Time evolution of transfer characteristic under typical NBTI stress for SPC TFTs with passivation layers before humidity treatment.

-n treated using hard bake again. After the hard bake, the same NBTI stress is used to another TFT when the wafer cools down to room temperature. As shown in Fig.2d is the time evolution of transfer characteristic under typical NBTI stress after hard bake treatment. Compared to the TFT with humidity treatment as shown in Fig.2c, both I_{on} and V_{th} are recovered a lot by the hard bake, which is also as shown in Fig.3. This is due to the moisture evaporation in the TFT structure as discussed above. Based on the above experiments, it can be concluded that the instability of LTPS TFTs after a period storage is related to moisture.

To prevent the moisture penetrating into the TFT structure, passivation layers of combined SiO_2 and Si_3N_4 are deposited on the top of poly-Si TFT structure are deposited in sequence using PECVD. As shown in Fig.4 is the time

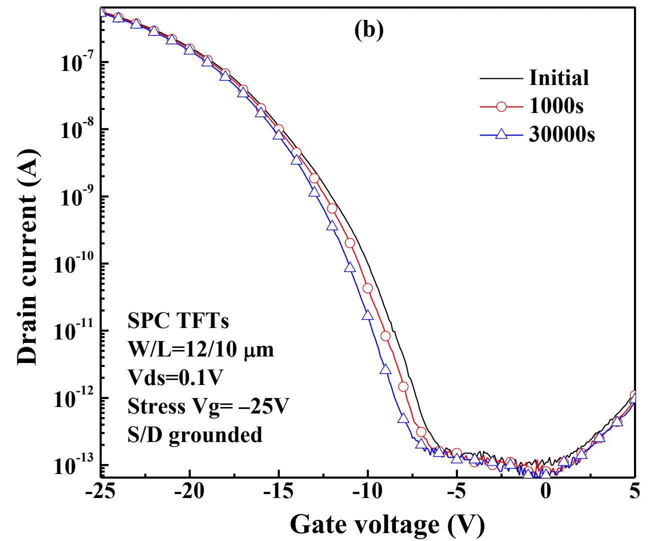

Fig.4 (b) Time evolution of transfer characteristic under typical NBTI stress for SPC TFTs with passivation layers after humidity treatment.

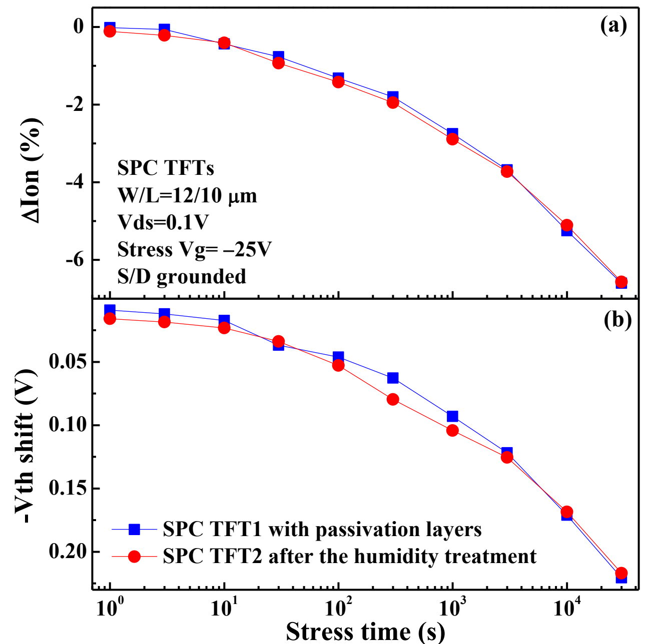

Fig.5: Before and after humidity treatment, dependence of (a) I_{on} degradation and (b) V_{th} shift on stress time for SPC TFTs with passivation layers under the typical NBTI stress.

evolution of transfer characteristic under typical NBTI stress for SPC TFTs with passivation layers before (Fig.4a) and after (Fig.4b) humidity treatment. It seems that almost the same NBTI degradation occurs with/without humidity treatment. Shown in Fig.5 is dependence of extracted I_{on} degradation (Fig.5a) and V_{th} shift (Fig.5b) on stress time for SPC TFTs with passivation layers under the typical NBTI stress. The NBTI degradation is almost the same, which indicates that the passivation layer can effectively keep the moisture from diffusing into the TFT structure and improve device reliability.

CONCLUSION

The instability of p-type LTPS TFTs after a period of storage is confirmed to be induced by the diffused moisture. Passivation layers at the top of TFT structure can

effectively protect the TFT from moisture penetration and improve device reliability.

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