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Self-aligned indium–gallium–zinc oxide thin-film transistors with $SiN_x/SiO_2/SiN_x/SiO_2$ passivation layers

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ABSTRACT

Self-aligned top-gate amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs) with $SiN_x/SiO_2/SiN_x/SiO_2$ passivation layers are developed in this paper. The resulting a-IGZO TFT exhibits high reliability against bias stress and good electrical performance including field-effect mobility of 5 cm^2/Vs, threshold voltage of 2.5 V, subthreshold swing of 0.63 V/decade, and on/off current ratio of 5×10^6. With scaling down of the channel length, good characteristics are also obtained with a small shift of the threshold voltage and no degradation of subthreshold swing. The proposed a-IGZO TFTs in this paper can act as driving devices in the next generation flat panel displays.

1. Introduction

Recently, amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs) have become attractive for use as driving devices in large scale active matrix organic light emitting diode (AMOLED) applications, due to their higher mobility and larger area uniformity, as compared to amorphous silicon (a-Si) and polycrystalline silicon (p-Si) TFTs [1–4]. The conventional a-Si TFTs, which are used as switching devices in active-matrix liquid–crystal display, have the advantages of low manufacturing cost and large area uniformity. However, their low field-effect mobility (<1 cm^2/Vs) may not be sufficient to drive AMOLED. Due to their high mobility (>50 cm^2/Vs) and electrical stability, the conventional p-Si TFTs are currently used as driving devices in AMOLED displays. But the main issues are the non-uniformity of their field-effect mobility and threshold voltage, caused by the grain size and grain boundaries in p-Si thin films.

Conventional bottom-gate structure is widely studied for a-IGZO TFTs. But this structure is unsuitable for the integration of peripheral circuits for the system on glass and realization of high resolution high quality AMOLED displays, due to the high parasitic capacitance and poor scalability. Therefore, the development of self-aligned top-gate oxide TFT with good performance and high stability is necessary for AMOLED display applications. For example, several self-aligned structure oxide TFTs were reported, in which source and drain were doped by hydrogen diffusion from silicon nitride by plasma enhanced chemical vapor deposition (PECVD) [5,6] or by plasma treatment [7,8]. But it needs additional process step for the source and drain doping. Passivation layer has a major effect on the long-term stability for a-IGZO TFTs. Single SiN_x layer deposited by PECVD has poor passivation ability for the oxygen or water penetration, which easily degrades the performance of a-IGZO TFTs [9].

In this paper, a self-aligned top-gate structure a-IGZO TFT with $SiN_x/SiO_2/SiN_x/SiO_2$ passivation layers has been developed. The source and drain were doped n-type during over-etch of the gate dielectric with CHF_3/O_2 plasma. The proposed a-IGZO TFTs show good electrical performance and high reliability against bias stress.

2. Experimental

The cross-sectional schematic of the self-aligned top-gate type a-IGZO TFT studied in this paper is shown in Fig. 1.

A 100 nm thick a-IGZO active layer was first sputtered on thermally oxidized silicon wafer by DC magnetron sputtering using a target of In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol% in a mixed argon and oxygen ambient at room temperature. The deposition pressure and the power were 0.27 Pa and 120 W, respectively. After patterning this a-IGZO active layer by lift-off process, a 120 nm thick SiO_2 layer as gate dielectric was deposited by PECVD from SiH_4 and N_2O precursors on top of the a-IGZO layer at 300 °C. The gas flows of SiH_4 and N_2O are 8 sccm and 1400 sccm, respectively. A 100 nm thick indium tin oxide (ITO), used as gate electrode, was sequentially sputtered at room temperature, and then defined by using photolithography and lift-off process. Then, the annealing process was executed at 200 °C for 30 min in a N_2 ambient. By reactive ion etching using CHF_3/O_2 plasma, the SiO_2 gate dielectric was then self-aligned dry etched using ITO gate electrode pattern as a mask. After that, $SiN_x/SiO_2/SiN_x/SiO_2$ multiple layers were deposited as passivation layers by PECVD at 150 °C. The deposition condition of SiO_2 is the same as that of the gate dielectric layer. The precursors for SiN_x deposition are SiH_4 and NH_3. The gas flows of SiH_4 and NH_3 are

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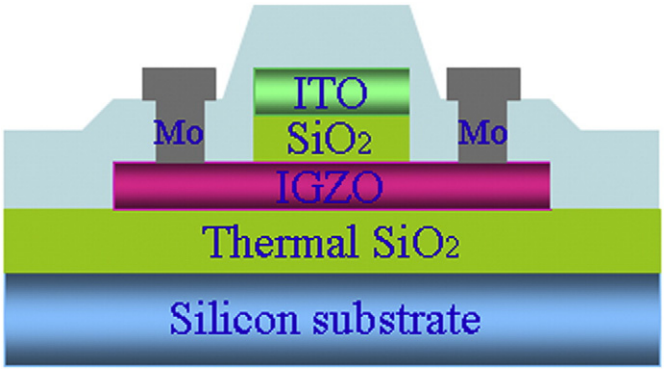

Fig. 1. A cross-section schematic of the proposed a-IGZO TFT with self-aligned top-gate structure.

40 sccm and 30 sccm, respectively. After forming the contact holes, a 200 nm thick Mo layer was deposited by sputtering and patterned as gate/source/drain electrodes. The electrical properties of the a-IGZO TFTs were measured by using an HP4156A precision semiconductor parameter analyzer.

3. Results and discussion

The field-effect mobility induced by the transconductance at a low drain voltage is given by

$$\mu_{FE} = \frac{Lg_m}{WC_{OX}V_{DS}} \quad (1)$$

where g_m and C_{OX} are the transconductance and the gate insulator capacitance per unit area, respectively. Fig. 2 shows the typical transfer and output characteristics of the fabricated a-IGZO TFTs with a width to length ratio of 30/16 μm. They exhibit good transfer TFT characteristics at a drain to source voltage (V_{DS}) of 0.2 V such as field-effect mobility of 5 cm^2/Vs, threshold voltage of 2.5 V, subthreshold swing of 0.63 V/decade and on/off current ratio of 5×10^6. The output characteristic shows clear linear regions and does not show significant current crowding at low V_{DS}, indicating that low series resistance in source/drain contacts was obtained.

Fig. 3(a) shows the dependence of the channel length (L) on the field-effect mobility of the a-IGZO TFTs. As the channel length decreased from 16 μm to 2 μm, the maximum field-effect mobility of the a-IGZO TFTs decreased from 5 to 2.2 cm^2/Vs. The decrease of the field-effect mobility for short channel devices is due to the existence of the source/drain series resistance R_{SD} on the potential distribution across the channel. Without considering this effect of R_{SD}, the field-effect mobility extracted using Eq. (1) underestimates the true field-effect mobility for the a-IGZO TFTs. In order to obtain the true field-effect mobility, the R_{SD} could be extracted by using the following relationship [10]:

$$\mu_{FE} \approx \mu_0 \frac{L}{L + \mu_0 WC_{OX}R_{SD}(V_{GS} - V_{th})} \quad (2)$$

where μ_{FE} is the apparent field-effect mobility and μ_0 is the true field-effect mobility of the a-IGZO material. The R_{SD} for the a-IGZO TFTs was extracted to be 115 kΩ from the fitting of the apparent field-effect mobility in Fig. 3(b) using Eq. (2). The width-normalized $R_{SD}W$ was 345 Ωcm. As a result, the true channel mobility was extracted to be 6.1 cm^2/Vs for the a-IGZO TFTs.

The R_{SD} was also extracted by determining the device on-resistance R_{on} from the linear region of the transfer characteristics and plotting the width normalized $R_{on}W$ as a function of the L for different gate voltages [11]. Fig. 4 shows the width normalized $R_{on}W$ as a function of L at different gate voltage at $V_{DS} = 0.2$ V for the a-IGZO TFTs. The $R_{SD}W$ for the a-IGZO TFTs, which is extracted at the y-axis intercept of the extrapolated linear fit of $R_{on}W$ versus L, is approximately 300 Ωcm for $V_{GS} = 10$ V,

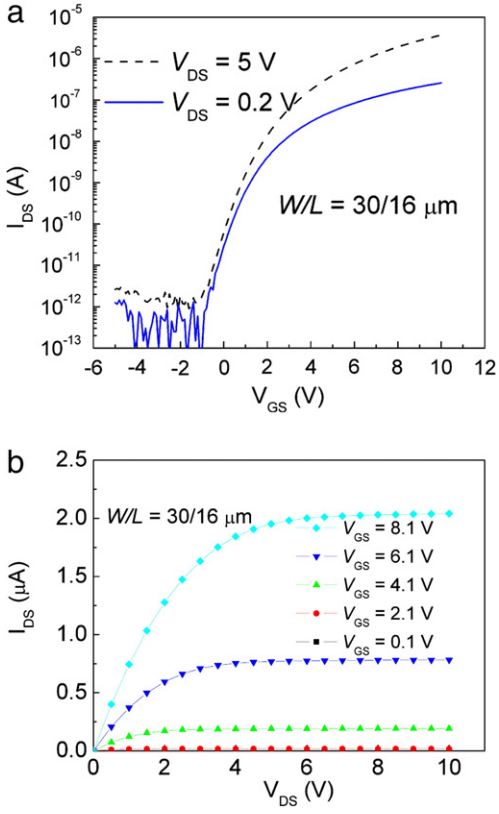

Fig. 2. (a) Transfer characteristic and (b) output characteristic of the proposed self-aligned top-gate a-IGZO TFTs.

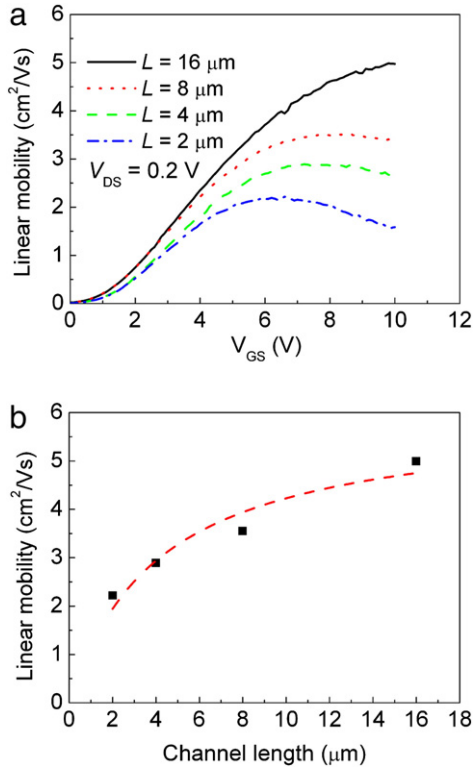

Fig. 3. (a) Dependence of channel length L on the field-effect mobility μ_{FE} for the a-IGZO TFTs. (b) The field-effect mobility μ_{FE} at various channel length L and the fitting result considering R_{SD} (red dash curve).

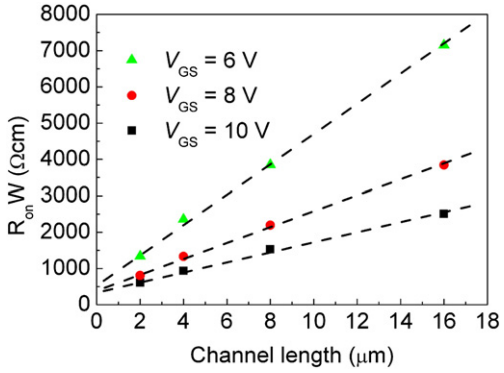

Fig. 4. Width normalized device on-resistance $R_{on}W$ as a function of L.

which is similar to that of bottom-gate a-IGZO TFTs [3]. The $R_{SD}W$ value extracted by this method is similar to that extracted from the fitting result in Fig. 3(b) using Eq. (2). This low source/drain series resistance is caused by the surface modification and hydrogen diffusion into source/drain area during over-etch of the gate oxide SiO_2 dry-etching process with CHF_3/O_2 plasma and silicon nitride deposition process with SiH_4 and NH_3 plasma. Hydrogen diffusion into the a-IGZO thin film can cause low resistivity of the a-IGZO. Hydrogen is an n-type dopant for a-IGZO thin film. The sheet resistance of a-IGZO thin film after dry-etching process of the gate oxide and deposition process of silicon nitride was found to be as low as 3 kΩ/sq. Different from earlier reports [7,8], no further plasma treatment process is needed for the source/drain area.

To study the short channel effects, the transfer characteristic (at V_{DS} = 5 V) of the a-IGZO TFTs with different channel lengths (L = 16, 8, 4, 2 μm) is compared in Fig. 5. From Fig. 5, a small change of the threshold voltages and no degradation of subthreshold swing with different channel lengths were obtained, which indicates good stability against short channel effects. This good scaling down behavior implicates small lateral diffusion of the hydrogen from the source/drain area to the channel region. This characteristic is much better than that reported earlier [6,12].

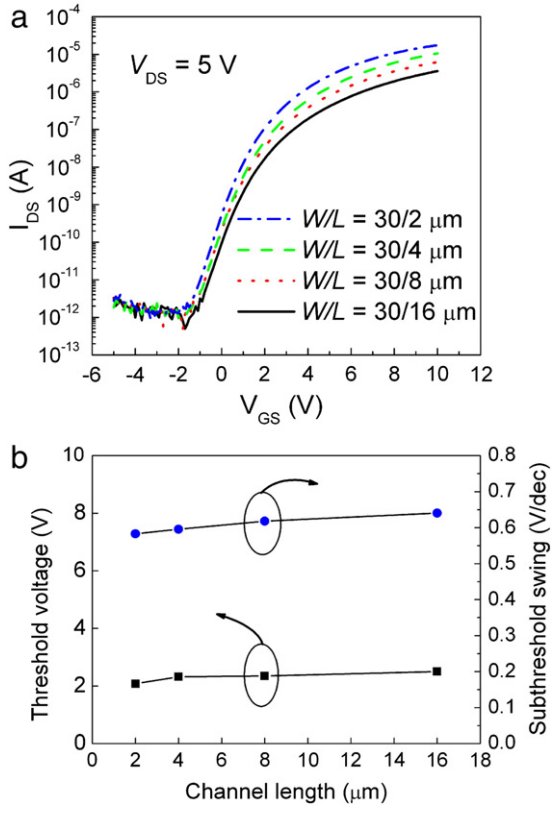

Fig. 5. (a) Transfer characteristics of the a-IGZO TFTs with the same channel width but different channel lengths. (b) Threshold voltage and subthreshold swing at various channel lengths for the a-IGZO TFTs.

To investigate the effect of SiO_2 gate dielectric and its interface with active layer, the hysteresis of *a*-IGZO TFT was examined, as shown in Fig. 6. A very small shift of threshold voltage for the hysteresis loop indicated that little electrons were trapped at or near the SiO_2/IGZO interface or within the a-IGZO channel layer.

Channel protection with passivation layer is crucial for improving the long-term stability of a-IGZO TFTs. Conventional single silicon nitride passivation layer deposited by PECVD easily degrades the a-IGZO TFTs performance due to its poor passivation ability for the oxygen or water penetration [9]. SiO_2 film deposited by PECVD has high barrier property and very low hydrogen content. Dielectric SiN_x or SiO_2 thin film deposited by PECVD at low temperature usually has pinhole defects inside the film, which will degrade the passivation quality of the film. The pinholes in one layer could be covered by another layer. The stack of four layers of $SiN_x/SiO_2/SiN_x/SiO_2$ has better passivation quality than one or two layers. Therefore, $SiN_x/SiO_2/SiN_x/SiO_2$ multiple layers were used as passivation layers in this work. Fig. 7 shows the shift of transfer characteristic of a-IGZO TFT after bias stress. The bias stress condition was set to two types of the constant current bias (I_{DS} = 2.1 μA), as shown in Fig. 7(a) and the negative gate bias (V_{GS} = −6 V, V_{DS} = 6 V), as shown in Fig. 7(b). From these two experiments, the shift of threshold voltage after 7200 s of both bias stress were below 0.4 V.

4. Conclusion

Self-aligned top-gate a-IGZO TFTs are developed in this paper. The resulting transistor exhibits field-effect mobility of 5 cm^2/Vs, threshold voltage of 2.5 V, subthreshold swing of 0.63 V/decade and on/off current ratio of 5×10^6. With scaling down the channel length, good characteristics are also obtained with small change of the threshold voltages and no degradation of subthreshold swing. Under constant current bias and negative gate bias stress, the shift of threshold voltage after 7200 s was below 0.4 V, due to good $SiN_x/SiO_2/SiN_x/SiO_2$ multiple passivation layers. The proposed top-gate a-IGZO TFTs in this paper can act as driving devices in the next generation flat panel displays.

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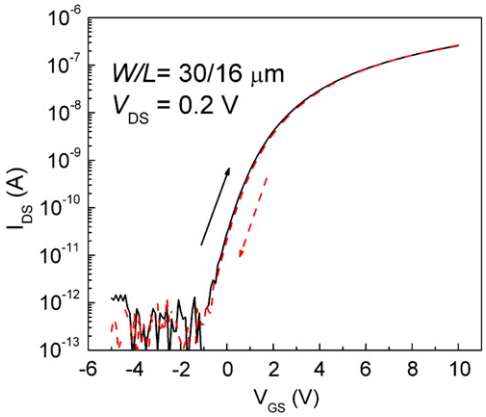

Fig. 6. Hysteresis characteristic of the a-IGZO TFTs.

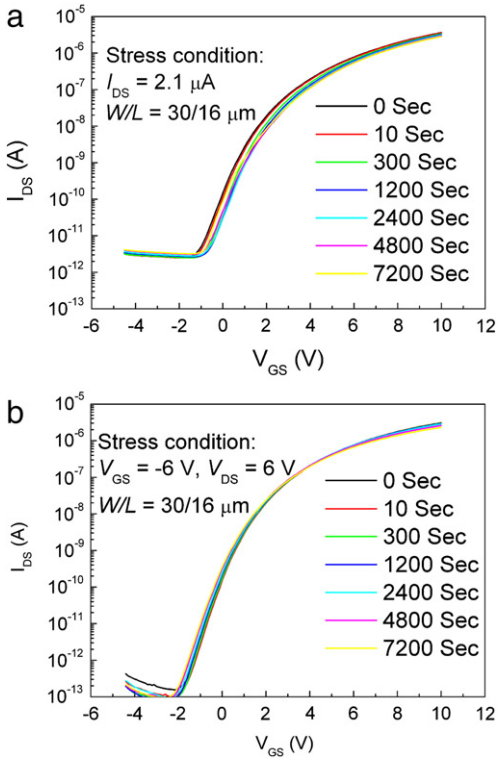

Fig. 7. Evolution of the transfer characteristics as a function of (a) constant current stress time and (b) negative gate bias stress time.

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