Geometric Effect Elimination and Reliable Trap State Density Extraction in Charge Pumping of Polysilicon Thin-Film Transistors

Lei Lu, Mingxiang Wang, *Senior Member, IEEE*, and Man Wong, *Senior Member, IEEE*

***Abstract*—The charge pumping (CP) technique in polysilicon thin-film transistors (TFTs) is optimized by adjusting the gate pulse transition times to eliminate the geometric component of the CP current. Improved CP curves similar to those in MOSFETs are obtained for polysilicon TFTs. Typical trap state density (D_t) energy distribution within the upper part of the band gap and the mean D_t value ($\overline{D}_t$) are reliably extracted in different approaches. Furthermore, based on the traditional CP model, a modified D_t extraction approach, where the influence of the CP geometric component is inherently avoided, is first proposed. Such an extracted $\overline{D}_t$ agrees well with those extracted by two optimized conventional approaches where geometric effect is eliminated.**

***Index Terms*—Charge pumping (CP), geometric effect, polysilicon, thin-film transistors, trap state density.**

I. Introduction

CHARGE pumping (CP) is a powerful technique to probe interface trap states for MOSFETs [1]–[5]. For polycrystalline-silicon (poly-Si) thin-film transistors (TFTs), it was also employed to characterize their trap state density (D_t) [6]–[12] or evaluate their degradation [13], [14]. Unlike in MOSFETs, however, CP in poly-Si TFTs never became a "standard" characterization technique. In previous studies, irregular distortion of CP Elliot curves [1], [2] was often observed [6], [10], and the extracted D_t energy distribution $D_t(E)$ was distorted [8], [9] and inconsistent to those obtained using other techniques [15]–[17]. Among the possible major causes are that those CP measurements in TFTs [8], [10] were not optimized and that the important geometric effect [1], [2], [5] was not eliminated.

In the CP measurement, during V_g pulse rising edge where an n-channel TFT is pulsed from accumulation to inversion, some free holes may have no enough time to flow back to the substrate. They will subsequently be recombined by channel inversion electrons from the source/drain (S/D). A similar process may also happen for the channel remaining electrons by the accumulated holes after pulse falling edge. It contributes

Manuscript received February 3, 2009; revised February 27, 2009. First published April 10, 2009; current version published April 28, 2009. This work was supported by the National Natural Science Foundation of China under Contract 60406001 and a Grant from the Research Grants Council of the HKSAR. The review of this letter was arranged by Editor A. Nathan.

L. Lu and M. Wang are with the Department of Microelectronics, Soochow University, Suzhou 215021, China (e-mail: Mingxiang_wang@suda.edu.cn).

M. Wong is with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Kowloon, Hong Kong.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2009.2017037

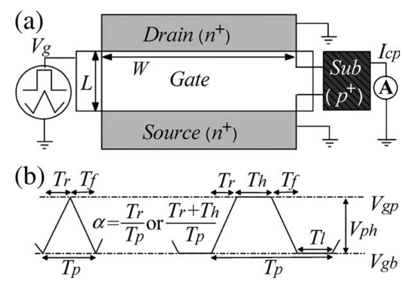

Fig. 1. (a) Device plane view and a schematic diagram of CP measurement. (b) Pulse parameter definition.

to the total recombined charges per cycle (Q_{ss}) and provides an additional component in the CP current (I_{cp}) besides the standard CP mechanism [1]–[3], i.e., the geometric current (I_{geo}) [1], [2], [5]. In the proposed CP technique, I_{geo} is minimized by adjusting the V_g transition times. Improved Elliot curves and typical $D_t(E)$ distribution for poly-Si TFTs are obtained. Finally, based on the traditional CP model, a modified D_t extraction approach where I_{geo} is readily excluded from I_{cp} is proposed. Such an extracted $\overline{D}_t$ agrees well with those extracted by two optimized conventional approaches.

II. CP Optimization for Geometric Effect Elimination

A poly-Si film is formed by solution metal-induced crystallization of a-Si at 630 °C for low-temperature (LT) devices and is recrystallized at 900 °C for high-temperature (HT) devices [18]. The measurement setup is shown in Fig. 1. Square or triangular V_g pulses are applied to n-channel TFTs $(W/L = 30/10\ \mu\mathrm{m})$, with the S/D being grounded. I_{cp} is measured from the p^+ diffused substrate side contact since there is no bottom contact. Pulse parameters include the pulse base/peak voltage $(V_{\mathrm{gb}}/V_{\mathrm{gp}})$, pulse height (V_{ph}), rising/falling time (T_r/T_f), high-/low-voltage duration (T_h/T_l), pulse period (T_p), and duty ratio $(\alpha = 0.5)$. Elliot CP curves are measured by sweeping V_{gb} while keeping a constant V_{ph} [1], [2].

In Fig. 2, Elliot curves are obtained using square pulses at different T_r/T_f's for a HT TFT. At $T_r = T_f = T_{r,f} = 0.1\ \mu$s, I_{cp} is the largest but is obviously distorted with a sharp peak that is largely shifted toward the negative. By symmetrically increasing $T_{r,f} \geq 1\ \mu$s, a regular CP curve appears, and the I_{cp} central region is flattened, similar to those in MOSFETs. In the inset, the I_{cp} peak current is plotted against $T_{r,f}$. I_{cp} increases with decreasing $T_{r,f}$, as expected [1], and an additional increase is observed when $T_{r,f} < 1\ \mu$s. Accordingly, the peak position

0741-3106/$25.00 © 2009 IEEE

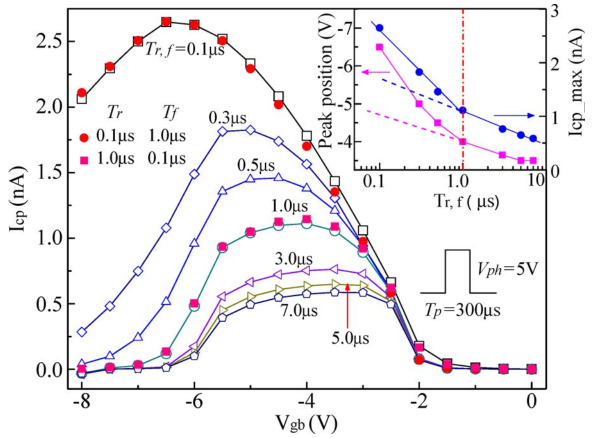

Fig. 2. Elliot curves for HT devices using square pulses with different T_r's and T_f's. The inset shows the peak position and $I_{\mathrm{cp\_max}}$ (the I_{cp} values at the corresponding peak positions) that are dependent on $T_{r,f}$. At $T_r > \sim 1\ \mu$s, I_{geo} is minimized, and improved CP curves are obtained.

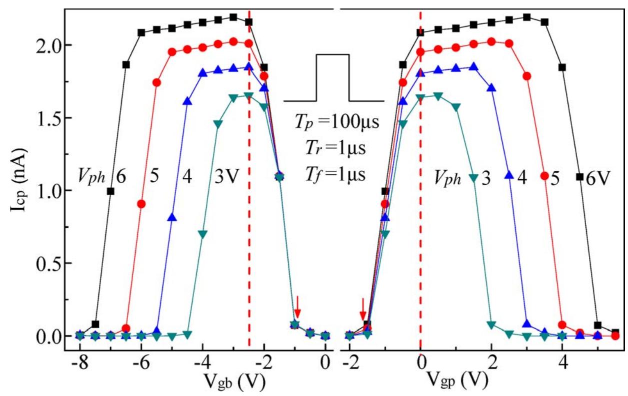

Fig. 3. Elliot curves for HT devices using optimized square pulses ($T_r = 1\ \mu$s for I_{geo} elimination) with different V_{ph}'s. I_{cp} is plotted against V_{gb} in the left and V_{gp} in the right. All curves are similar to those in MOSFETs. In addition, falling/rising edges and positions of central flat regions coincide.

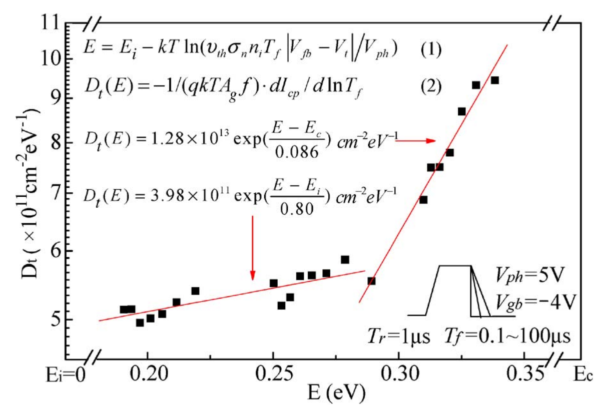

Fig. 4. Typical dual exponential $D_t(E)$ distribution between the midgap (E_i) and the conduction band (E_c) for HT devices extracted with (1) and (2) using optimized square pulses.

shift also follows the same characteristic. A critical $T_{r,f} \approx 1\ \mu$s can be estimated separating the two regions. It implies that an additional mechanism is involved in the I_{cp} current. In poly-Si TFTs, the hole transport from the channel region to the substrate contact is via a lateral path through the substrate bulk. With the presence of grain boundaries, a much longer transit time than that in MOSFETs is needed [8]. During V_g rising edge transient, some accumulated holes have no enough time to transit to the substrate side contact, so they remain in the channel when the channel is pulsed into inversion. Therefore, I_{geo} arises at small $T_{r,f}$ from the recombination of the remaining holes with inversion electrons from the S/D, causing the observed additional I_{cp} increase. Also, in Fig. 2, Elliot curves measured with asymmetric pulses ($T_r/T_f = 0.1/1$ or $1/0.1\ \mu$s, solid symbols) are compared with those with symmetric ones ($T_{r,f} = 0.1$ or $1\ \mu$s). Keeping $T_f = 0.1$ or $1\ \mu$s and increasing T_r from $0.1\ \mu$s to $1\ \mu$s dramatically reduce I_{cp}, while decreasing T_f only slightly increases I_{cp}. The correlation of I_{geo} suppression with longer T_r instead of T_f indicates the hole-transport-limited mechanism for I_{geo}. The hole-related I_{geo} also explains the additional negative shift of I_{cp} peak position. When V_{gb} is more negative, the accumulated holes, as well as the channel remaining holes, increase, leading to a larger I_{geo} component. Here, the hole transit time is estimated as $\sim 1\ \mu$s, while the electron transit time $< 0.1\ \mu$s. The I_{geo} component can be minimized by setting $T_r \geq 1\ \mu$s. In MOSFETs, the CP geometric effect is suppressed by using a device that has $W/L > 1$ or with a short-enough L [2], which is clearly not true in poly-Si TFTs.

Shown in Fig. 3 are Elliot curves measured using optimized square pulses ($T_r = 1\ \mu$s for I_{geo} suppression) at different V_{ph}'s, which are plotted against V_{gb} (left) or V_{gp} (right). With I_{geo} being eliminated from I_{cp}, improved Elliot curves with clearly converged falling/rising edge ($V_{\mathrm{gb}} \approx -1$ V or $V_{\mathrm{gp}} \approx -1.5$ V) and central flat region ($V_{\mathrm{gb}} \leq -2.5$ V and $V_{\mathrm{gp}} \geq 0$) are obtained. The maximum I_{cp} is seen to gradually increase with V_{ph}, agreeing with a previous CP model [1], [6]. With curve distortion [6], [10] being removed, the optimized CP measurement is clearly more suitable for reliable D_t extraction in poly-Si TFTs.

III. Reliable D_t Extraction

$D_t(E)$ distribution can be extracted from the transition time dependence of I_{cp} using square pulses following the equations shown in Fig. 4 [1]. With fixed $T_r = 1\ \mu$s but varying T_f, one extracts D_t at the corresponding energy levels between the conduction band (E_c) and the midgap (E_i). In Fig. 4, the D_t that is extracted on a HT TFT follows a dual exponential distribution, well agreeing with typical D_t distribution in poly-Si TFTs determined by other techniques [15]–[17]. This result is in contrast to the distorted distribution obtained in previous studies [8], [9].

Traditionally, an average $D_t(\overline{D}_t)$ is extracted from the frequency dependence of I_{cp} using square pulses (I_{cp} approach) or of Q_{ss} using triangular pulses ($T{-}Q_{\mathrm{ss}}$ approach) [1]. However, the I_{cp} approach is not independent because, in the extraction equation [see Fig. 5, eq. (3)], the capture cross section $(\sigma_n\sigma_p)^{1/2}$ still needs to be estimated by the $T{-}Q_{\mathrm{ss}}$ approach. Here, an $S{-}Q_{\mathrm{ss}}$ approach is proposed using the $T_{r,f}$ dependence of Q_{ss} measured with symmetrical square pulses. In (3), using $T_r = T_f = T_{r,f}$ and $Q_{\mathrm{ss}} = I_{\mathrm{cp}}/f$, one obtains $Q_{\mathrm{ss}} = 2qkTA_g\overline{D}_t[\ln T_{r,f} + \ln(\upsilon_{\mathrm{th}}n_i|V_t - V_{\mathrm{fb}}|/V_{\mathrm{ph}}\sqrt{\sigma_n\sigma_p})]$ (4). Therefore, in the semilog plot of Q_{ss} versus $T_{r,f}$, a straight line is expected, with $\overline{D}_t$ and $(\sigma_n\sigma_p)^{1/2}$

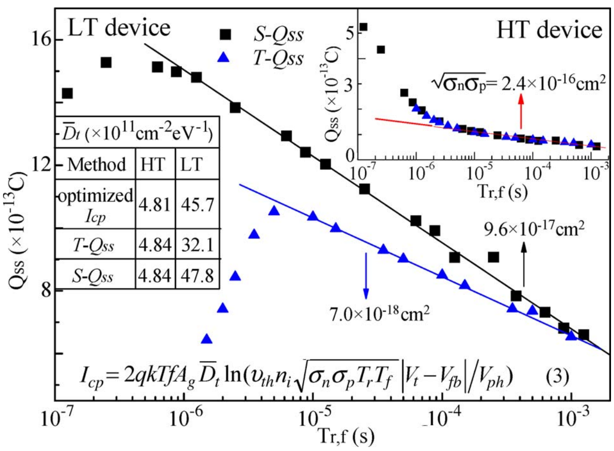

Fig. 5. Semilog plot of $Q_{\rm ss}$ versus $T_{r,f}$ using the $S-Q_{\rm ss}$ ($T_h = T_l = 100\ \mu$s) or $T-Q_{\rm ss}$ approach for HT (shown in the inset, $V_{\rm gb}/V_{\rm ph} = -4/5$ V) and LT ($V_{\rm gb}/V_{\rm ph} = -12/18$ V) devices. The slope and intercept of linear dependence are used to extract $\overline{D}_t$ and $(\sigma_n\sigma_p)^{1/2}$ using $2qkTA_g\overline{D}_t = (dQ_{\rm ss}/d\ln T_{r,f})$ and $(\sigma_n\sigma_p)^{1/2} = (T_0 v_{\rm th} n_i)^{-1}V_{\rm ph}/|V_{\rm fb} - V_t|$, respectively. $\overline{D}_t$ values by three approaches are compared. Furthermore, (3) is given.

being extracted from its slope and intercept (T_0) at $Q_{\rm ss} = 0$, respectively. The applicability of the $S-Q_{\rm ss}$ approach is demonstrated for both HT and LT TFTs in Fig. 5. Also plotted are data from the $T-Q_{\rm ss}$ approach, where traditional frequency dependence [1] is transformed to $T_{r,f}$ dependence using $f = 1/2T_{r,f}$. With the same substitution, one notes that the $T-Q_{\rm ss}$ extraction equation [1, Eq. (22)] is actually equivalent to (4) for the $S-Q_{\rm ss}$ method.

As shown in the inset for HT TFTs, indeed, data from $T-Q_{\rm ss}$ and $S-Q_{\rm ss}$ approaches overlap. The extracted $\overline{D}_t$'s from three approaches agree well. Deviation from linear dependence at $T_{r,f} \leq 2\ \mu$s is attributed to the $I_{\rm geo}$ component, as shown in Fig. 2. However, for LT TFTs, $Q_{\rm ss}$ drops quickly at short $T_{r,f}$. To form $I_{\rm cp}$ under dynamic V_g, the onset voltage of steady-state carrier capture (V_c) depends on the surface potential sweeping rate [3], which is much lower in LT TFTs due to the gradual subthreshold region [17]. With decreasing $T_{r,f}$, V_c moves from $V_t/V_{\rm fb}$ closer to $V_{\rm gp}/V_{\rm gb}$; hence, the carrier capture time is shortened by excluding T_r/T_f transitions [3]. Within the reduced capture time, a larger percentage of deep traps will not participate in the carrier capture process and do not contribute to $Q_{\rm ss}$ [3]. Both effects cause the observed $Q_{\rm ss}$ drop at small $T_{r,f}$ [1], [3]. Apparently, the $T-Q_{\rm ss}$ approach is more affected by such effects since triangular pulses have no T_h/T_l; hence, the measured $Q_{\rm ss}$ is lower than that of the $S-Q_{\rm ss}$ approach and drops more sharply and earlier. With more accurate $Q_{\rm ss}$ data in a wider range being obtained, the proposed $S-Q_{\rm ss}$ approach should be more reliable for trap characterization. Indeed, the extracted $\overline{D}_t$ and $(\sigma_n\sigma_p)^{1/2}$ values are more consistent in the $S-Q_{\rm ss}$ approach, as shown in Fig. 5, while they are underestimated in the $T-Q_{\rm ss}$ approach.

IV. Conclusion

CP is optimized to minimize $I_{\rm geo}$ in poly-Si TFTs by adjusting the gate pulse transition times. Based on optimization, improved Elliot curves and typical dual exponential D_t distribution are obtained. In addition, a reliable D_t extraction method is proposed, where the extracted $\overline{D}_t$ agrees well with those obtained from two optimized traditional approaches in both HT and LT TFTs. Both optimization and the proposed extraction method make the CP technique more reliable for trap characterization in poly-Si TFTs.

References

[1] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, no. 1, pp. 42–53, Jan. 1984.

[2] C. R. Viswanathan and V. Ramgopal Rao, "Application of charge pumping technique for sub-micron MOSFET characterization," *Microelectron. Eng.*, vol. 40, no. 3, pp. 131–146, Nov. 1998.

[3] D. Bauza, "Rigorous analysis of two-level charge pumping: Application to the extraction of interface trap concentration versus energy profiles in metal–oxide–semiconductor transistors," *J. Appl. Phys.*, vol. 94, no. 5, pp. 3239–3248, Sep. 2003.

[4] C. Wenliang, A. Balasinski, and T.-P. Ma, "A charge pumping method for rapid determination of interface-trap parameters in metal–oxide–semiconductor devices," *Rev. Sci. Instrum.*, vol. 63, no. 5, pp. 3188–3190, May 1992.

[5] G. Van den Bosch, G. Groeseneken, and H. E. Maes, "On the geometric component of charge-pumping current in MOSFETs," *IEEE Electron Device Lett.*, vol. 14, no. 3, pp. 107–109, Mar. 1993.

[6] M. Koyanagi, I.-W. Wu, A. G. Lewis, M. Fuse, and R. Bruce, "Evaluation of polycrystalline silicon thin film transistors with the charge pumping technique," in *IEDM Tech. Dig.*, 1990, pp. 863–866.

[7] M. Koyanagi, Y. Baba, K. Hata, I.-W. Wu, A. G. Lewis, M. Fuse, and R. Bruce, "The charge-pumping technique for grain boundary trap evaluation in polysilicon TFTs," *IEEE Electron Device Lett.*, vol. 13, no. 3, pp. 152–154, Mar. 1992.

[8] G.-W. Lee, J.-W. Lee, and C.-H. Han, "Substrate resistance effect on charge-pumping current in polycrystalline silicon thin film transistors," *Jpn. J. Appl. Phys.*, vol. 38, no. 4B, pp. 2656–2659, Apr. 1999.

[9] K.-J. Kim and O. Kim, "Identification of grain-boundary trap properties using three-level charge-pumping technique in polysilicon thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 36, no. 3B, pp. 1394–1397, Mar. 1997.

[10] N. S. Saks, S. Batra, and M. Manning, "Charge pumping in thin film transistors," *Microelectron. Eng.*, vol. 28, no. 1–4, pp. 379–382, Nov. 1995.

[11] K.-J. Kim, W.-K. Park, S.-G. Kim, K.-M. Lim, I.-G. Lim, and O. Kim, "A new charge pumping model considering bulk trap states in polysilicon thin film transistor," *Solid-State Electron.*, vol. 42, no. 11, pp. 1897–1903, Nov. 1998.

[12] O. Kim and K.-J. Kim, "Charge pumping investigations on parasitic regions in polysilicon TFT," *Electron. Lett.*, vol. 34, no. 8, pp. 809–811, Apr. 1998.

[13] A. Balasinski, J. Worley, M. Zamanian, and F. T. Liou, "Reference voltages and their stress-induced changes in thin film transistors as determined by charge pumping," in *IEDM Tech. Dig.*, 1995, pp. 529–532.

[14] C.-Y. Chen, M.-W. Ma, W.-C. Chen, H.-Y. Lin, K.-L. Yeh, S.-D. Wang, and T.-F. Lei, "Analysis of negative bias temperature instability in body-tied low-temperature polycrystalline silicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 29, no. 2, pp. 165–167, Feb. 2008.

[15] L. Pichon, A. Boukhenoufa, C. Cordier, and B. Cretu, "Determination of interface state distribution in polysilicon thin film transistors from low-frequency noise measurements: Application to analysis of electrical properties," *J. Appl. Phys.*, vol. 100, no. 5, p. 054 504, Sep. 2006.

[16] G. A. Armstrong, S. Uppal, S. D. Brotherton, and J. R. Ayres, "Differentiation of effects due to grain and grain boundary traps in laser annealed poly-Si thin film transistors," *Jpn. J. Appl. Phys.*, vol. 37, no. 4A, pp. 1721–1726, Apr. 1998.

[17] H. Ikeda, "Evaluation of grain boundary trap states in polycrystalline-silicon thin-film transistors by mobility and capacitance measurements," *J. Appl. Phys.*, vol. 91, no. 7, pp. 4637–4645, Apr. 2002.

[18] B. Zhang, Z. Meng, S. Zhao, M. Wong, and H.-S. Kwok, "Polysilicon thin film-transistors with uniform and reliable performance using solution-based metal-induced crystallization," *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp. 1244–1248, May 2007.