Evaluation of Self-Heating and Hot Carrier Degradation of Poly-Si Thin-Film Transistors using Charge Pumping technique

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***Abstract*—Self-heating (SH) and hot carrier (HC) degradation of n-type poly-Si thin-film transistors (TFTs) is evaluated by using charge pumping (CP) technique. By extracting trap state energy distribution, it is demonstrated that SH degradation is mainly attributed to the generation of deep states. For HC stressed TFTs, an anomalous I_{CP} decrease with the stress time is observed in a low V_g stress condition controlled by hole trapping; while in a mid V_g condition, CP signal clearly indicates the trap states generation controlled by electron trapping.**

Keywords: charge pumping, poly-Si TFTs, self-heating, hot carrier

I. INTRODUCTION

Charge pumping (CP) is a technique providing direct information on interface trap properties [1], and has been extensively employed to investigate device degradation in MOSFETs [2]. While in poly-Si thin-film transistors (TFTs), there are very limited applications of CP for hot carrier (HC) or NBTI degradation [3, 4]. Recently, we showed that measurement optimization was critical to achieve reliable CP characterization in poly-Si TFTs [5]. In this work, such optimized CP technique is employed to evaluate their self-heating (SH) and HC degradation. For SH degradation, trap states generation mainly on the deep states is observed. While for HC degradation, different CP characteristics are observed in low and mid V_g stress conditions. An abnormal I_{CP} decrease with the stress time is observed in low V_g stressed TFTs, which is different from previous observations [3], whereas in mid V_g stressed TFTs, CP characterization clearly indicates the electron trapping dominated trap states generation.

II. EXPERIMENTAL

N-type TFT with a p^+ side contact connecting the poly-Si body is used in this study. As shown in Fig.1a is a planar view of the device under test. The 100 nm poly-Si active layer was formed by solution based metal-induced crystallization of a-Si. Wafers were first dipped in nickel nitrate solution, and then crystallized at 630 °C in N_2 ambient. Subsequently the poly-Si film was recrystallized at 900 ºC. Gate oxide was formed by polyoxidation at 950 ºC in dry O_2 for 48 mins. Phosphorous implantation was introduced to form the source and drain with a dose of 4×10^{15} cm^{-2}, then followed by a dopant activation at 900 °C for 1.5 h. Device W/L for SH stress test is 15/4 μm while for HC stress is 10/4 or 20/4 μm. For SH stress, V_g/V_d=12/14 V is applied with a stress power about 47 mW. For HC stress, low V_g and mid V_g stress are applied with bias stress of V_g/V_d =2/10 V and 6/12 V, respectively.

Fig.1b is a cross sectional view of CP measurement. All stress test and CP measurement are performed at room temperature. Before and after a HC or SH stress, the TFT is pulsed from accumulation to inversion using a square V_g pulse with the source (S) and drain (D) grounded. By adjusting the pulse base voltage (V_{gb}) while keeping a constant pulse height (V_{ph}), an Elliot curve is measured from the p^+ side contact [1, 5] for CP analysis. In the CP measurement, the pulse period (T_p) is 100 μs and V_{ph} is fixed at 5 V. The pulse rising and falling time (T_r, T_f) are chosen as 5 μs, long enough to minimize the geometric effect [5]. Thus reliable and well shaped CP curves can be obtained. Besides, transfer curves are also measured before and after the degradation by using Agilent 4156C analyzer and Vector MX-1100B prober.

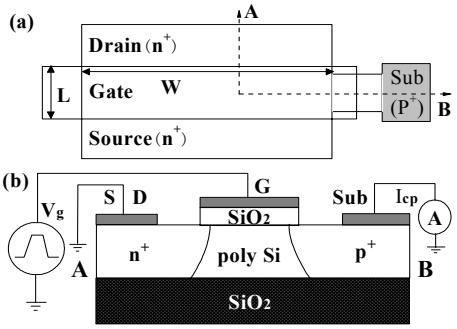

Figure 1. (a). Planar view of the high temperature processed TFT under test. (b). Cross sectional view of CP measurement.

III. RESULTS AND DISCUSSIONS

SH Degradation

Shown in Fig.2 is typical transfer curve degradation of a SH stressed TFT [6]. The subthreshold slope degrades slightly, resulting in a positive shift of device V_{th}. On current (I_{on}) decreases while leakage current (I_{off}) increases. In Fig.3 the Elliot curves measured at different stress times are shown. Clearly, CP current (I_{CP}) significantly increases with stress time, indicating the generation of interface traps. However, almost no shift in the Elliot curves is observed at either transition edge. Thus there should be no net charge generated in the gate oxide during the stress.

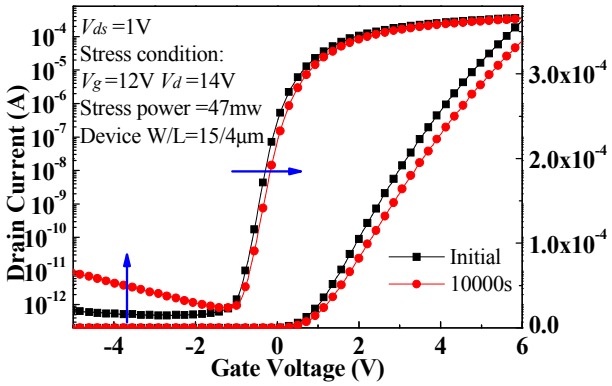

Figure 2. Linear and logarithmic plots of the typical transfer curves under SH stress, V_g/V_d=12/14 V, with a stress power of about 47 mw.

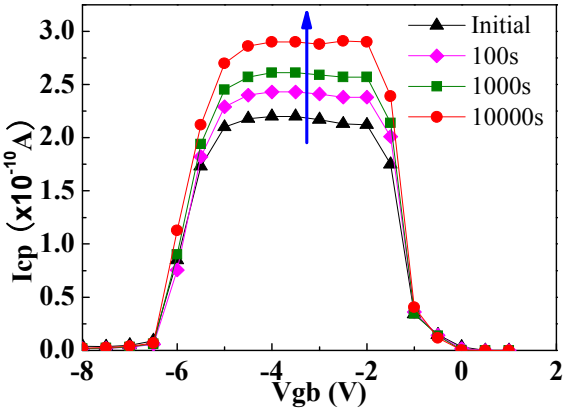

Figure 3. Charge pumping characteristics as a fucntion of pulse base voltage at various stress times. Distinct increase of I_{CP} is observed.

In Fig.4 inset, the maximum I_{CP} linearly increases with the measurement pulse frequency f, from which average trap densities (D_t) are extracted for all stress times using the equation [1] as below:

$$Icp = 2D_t[\ln(V_{th}n_i\sqrt{\sigma_n\sigma_p}) + \ln(\frac{|V_{fb}-V_t|}{V_{ph}}\sqrt{T_rT_f})]kTAgqf \quad (1)$$

The capture cross section $(\sigma_n\sigma_p)^{1/2}$ is set as 2.4×10^{-16} cm^2 [5]. Shown in Fig.4 is the extracted D_t as a function of stress time. In Fig.5 normalized degradation curves for key device parameters as well as D_t are compared. All curves follow a power law dependence on the stress time with about the same time exponent of 0.21, showing the correlation between the device degradation and trap states generation.

Furthermore, by measuring I_{CP} with fixed T_r and variable T_f, trap energy distribution $D_t(E)$ within the upper half of the band gap for each stress time can be extracted using the equation [1]:

$$D_t(E) = -\frac{T_f}{qfAgkT}\frac{dIcp}{dT_f} \quad (2)$$

In Fig.6 both deep states and tail states are seen to steadily increase with stress time, however, larger increase is observed near the mid-gap than that near the band edge. Deep states are normally attributed to dangling bonds due to bond breaking, while tail states to strained bonds [6]. Thus the observation here is a direct evidence to the SH trap generation mechanism related to Si-H or Si-Si breaking at the Si-SiO_2 interface or grain boundaries. In previous studies [7, 8], the same mechanism was proposed based on simulation or indirect observations, to which such direct CP evidence can be a better support. On the other hand, it also demonstrates the feasibility of the CP technique in probing the trap states generation in SH degraded poly-Si TFTs.

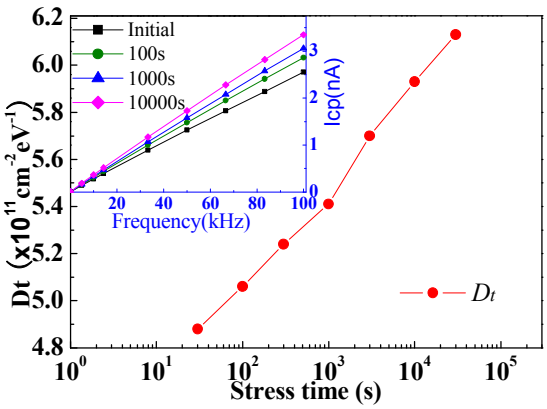

Figure 4. Stress time dependence of trap state density (D_t). The inset is frequency dependence of CP current, where average D_t can be extracted by the given equation (1).

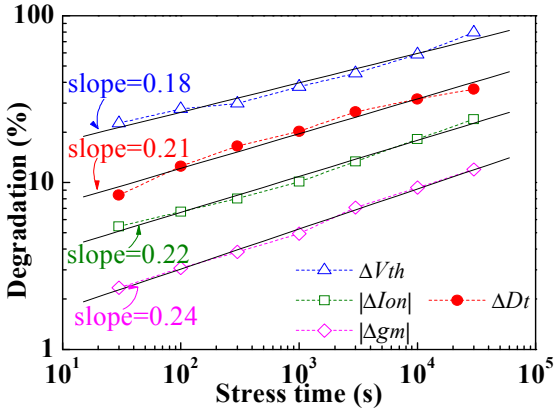

Figure 5. Stress time dependence of key device parameters degradation. D_t and device parameters follow a power law with about the same time exponent of 0.21.

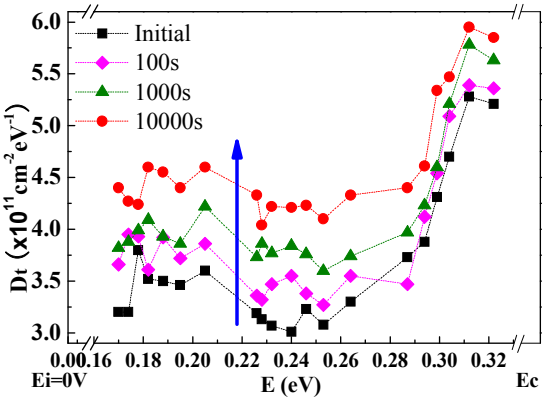

Figure 6. Trap state energy distribution $D_t(E)$ is extracted by keeping pulse T_r constant and varying T_f. SH degradation is mainly attributed to the generation of deep states.

HC Degradation

Shown in Fig.7 is transfer curve degradation of a low V_g HC stressed TFT. The subthreshold region continuously shifts to the negative and degrades severely. I_{off} increases distinctly, whereas negligible change occurs in I_{on}. Similar transfer curve degradation was also seen in other high temperature processed TFTs under similar low V_g HC stress condition [9]. Shown in Fig.8 are CP curves similarly measured by optimized CP technique as in SH degradation. The right edge of the Elliot curve clearly shifts to the negative, in accordance with the negative shift of the subthreshold region in Fig.7, indicating the generation of positive charges in the gate oxide [2]. Indeed, hot hole injection into the gate oxide is favored under a low V_g HC stress condition [2]. Surprisingly, I_{CP} clearly *decreases* with the stress times. It's a different observation from previous CP result also in low V_g HC stressed TFTs [3]. In order to verify such observation, pulse T_r and T_f is varied from 100 ns to 500 µs, all measured I_{CP} similarly decreases, eliminating the possibility of CP measurement error.

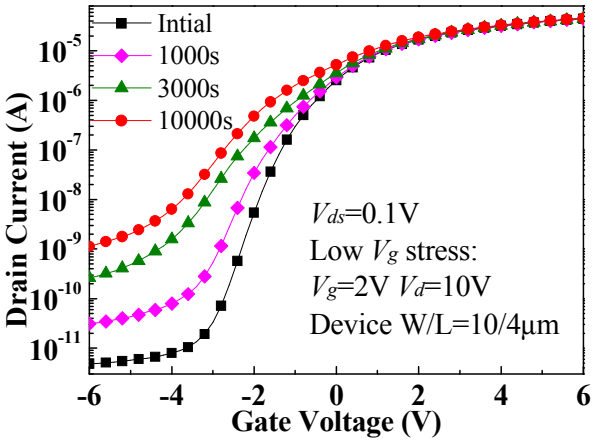

Figure 7. Stress time dependence of transfer curves under low V_g HC stress, V_g/V_d=2/10 V. Device W/L=10/4 µm.

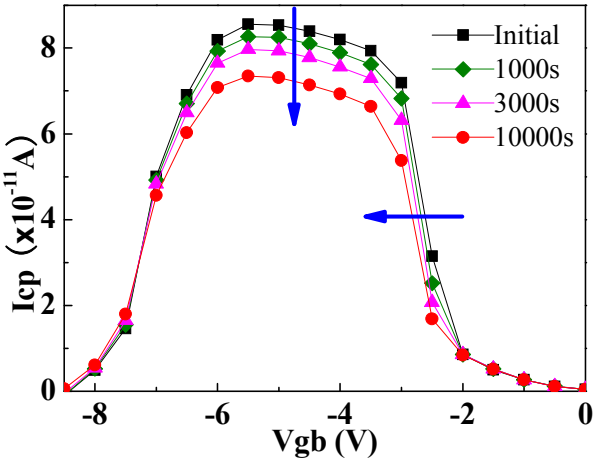

Figure 8. Charge pumping current versus pulse base voltage of the device under a low V_g HC stress.

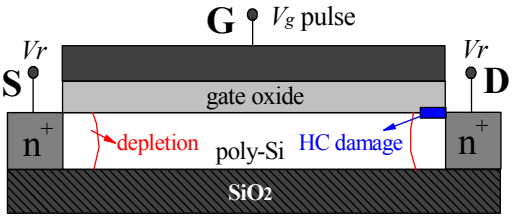

Figure 9. Schematic cross-sectional view of device in CP measurement. HC induced damage region can be masked by drain depletion region due to applied reverse bias V_r.

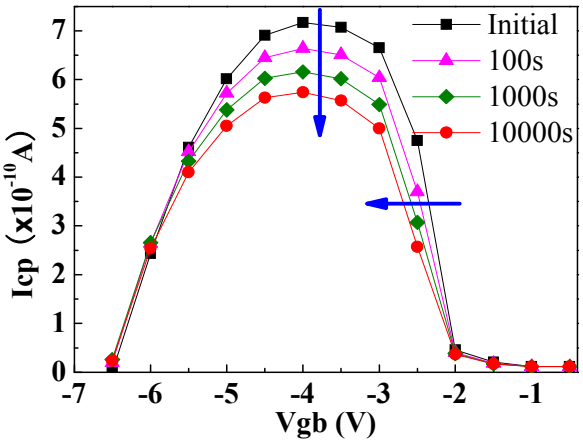

Figure 10. Charge pumping characteristics of device under a low V_g HC stress measured with the source and drain reversely biased at V_r=1 V.

Obviously, a conclusion of interface trap reduction based on the observed I_{CP} decrease can not be true. Thus one may consider that the effective channel length shortening due to HC injection into the gate oxide [2] may cause an I_{CP} reduction. To clarify this point, CP curve is measured with the source and drain reversely biased at V_r=1V, as shown in Fig.9. In such condition, HC induced damaged region [6] or HC injection induced local inversion region [2] at the drain end can be masked by a wider drain depletion region. Therefore, only the central channel region is probed by CP. As expected, such measured I_{CP} is reduced compared to that with S/D grounded, which is attributed to the reduction of effective gate area (A_g) as given in Eq.(1). However, the continuous I_{CP} decrease with the stress time still remains as shown in Fig.10. Thus we tend to believe that conventional I_{CP} measurement is not sensitive to the HC trap states generation dominated by hole trapping mechanism [10].

In a mid V_g HC stress condition, interface traps are generated through both electron and hole trapping [2]. Fig.11 is transfer curve degradation of a TFT stressed at V_g/V_d=6/12 V. In the inset, a positive shift of the right edge of the Elliot curve indicates the generation of net negative charges due to more electron trapping. Interestingly, here I_{CP} clearly *increases* with stress time, in agreement with the HC induced trap generation. Therefore, in both cases of HC degradation of poly-TFTs, shift of CP Elliot curve is a good indication of the respective trap generation mechanism, while one should be tentative when quantitatively evaluating trap generation using the I_{CP} variation. However, further investigation is needed to clarify the origin of the anomalous CP decrease under a low V_g HC stress.

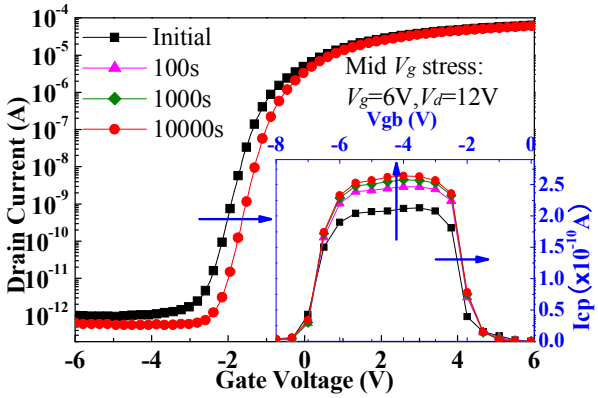

Figure 11. Transfer curve degradation of device under a mid V_g HC stress, V_g/V_d=6/12 V. Inset is degradation of CP characteristics, indicating the electron trapping dominated trap states generation. Device W/L=20/4 μm.

IV. CONCLUSION

The optimized CP technique was employed to evaluate the self-heating and hot-carrier degradation in poly-Si TFTs. SH degradation is mainly attributed to the generation of deep states. For HC degradation, CP exhibits different behaviors associated with different trap generation mechanisms. In the low V_g stress condition, the anomalous I_{CP} decrease is in contradiction to the HC trap states generation. While for the mid V_g HC stress induced degradation, CP characterization clearly indicates the electron trapping dominated trap states generation.

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