

# A New Observation of the Elliot Curve Waveform in Charge Pumping of Poly-Si TFTs

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**Abstract**—In the charge pumping (CP) measurement of poly-Si thin-film transistors (TFTs), the Elliot curve is found to be irrelevant to the flat-band voltage ( $V_{fb}$ ) and threshold voltage ( $V_{th}$ ) and hence does not follow the traditional MOSFET CP rule. Instead, a new correspondence between the TFT Elliot curve and device key parameters is observed. The critical onset voltages of the CP current are the threshold gate voltages for channel inversion and accumulation, which can be experimentally extracted by capacitance–voltage measurement. They are consistent with the general CP model and reduce to  $V_{fb}$  and  $V_{th}$  in MOSFETs.

**Index Terms**—Charge pumping (CP), Elliot curve, poly-Si, thin-film transistors (TFTs).

## I. INTRODUCTION

**C**HARGE pumping (CP) is a standard technique to evaluate the interface trap state density ( $D_t$ ) in MOSFETs [1]–[3]. When CP currents ( $I_{cp}$ ) are measured against the step increased gate pulse base voltage ( $V_{gb}$ ) with a fixed pulse height ( $V_{ph}$ ), an Elliot curve is obtained [1]. Ideally, its waveform is cap shaped with a central plateau and two steep transition edges at  $V_{gb} \approx V_{th} - V_{ph}$  and  $V_{fb}$  [see Fig. 1(a)]. The constant  $I_{cp}$  is normally used to calculate  $D_t$  with its onset  $V_g$ 's, i.e.,  $V_{fb}$  and  $V_{th}$  as extraction parameters [1]. Moreover, Elliot curves are also used to investigate the device degradation [2]. However, their waveforms in poly-Si thin-film transistors (TFTs) were far from ideal, which previously was ascribed to the fabrication process [4] or some unknown traps [5]. It prevents the clarification of the correspondence between the device characteristics and the Elliot curve. Thus, the traditional MOSFET CP rule was still followed in poly-Si TFTs [4]–[8].

Recently, it was revealed that the geometric effect largely affects the Elliot curve waveforms in poly-Si TFTs. Once it is minimized [10], regular cap-shaped Elliot curves can be reliably obtained. However, the transition edges are irrelevant to  $V_{fb}$  or  $V_{th}$ , indicating the invalidity of the MOSFET rule

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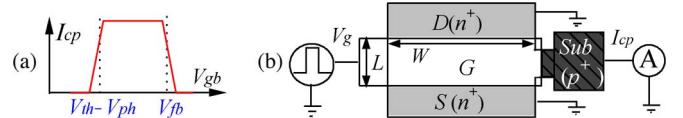


Fig. 1. (a) Correspondence rule for the MOSFET Elliot curve. (b) Planar view of an n-channel poly-Si TFT ( $W/L = 30/10 \mu\text{m}$ ) under CP test.

for TFTs. Moreover, the transition edges are not steep at all. Thus, it is more reasonable that each edge corresponds to two different  $V_g$  values at the start and end points, respectively. In this letter, such a correspondence between the Elliot curve and TFT characteristics is first observed. It provides one a better understanding of the Elliot curve in TFTs and a feasible tool for characterizing poly-Si TFTs and their degradation. Moreover,  $D_t$  can be more accurately extracted using corrected onset  $V_g$ 's.

## II. ELLIOT CURVES IN Poly-Si TFTs

The planar view of an n-channel poly-Si TFT under CP test is illustrated in Fig. 1(b). For low-temperature (LT) TFTs, poly-Si was formed by the solution-based metal-induced crystallization [11] of a-Si at 630 °C, while for high-temperature (HT) devices, an additional recrystallization was done at 900 °C.  $V_g$  pulses are applied with the source (S) and drain (D) grounded, and  $I_{cp}$  is measured from p<sup>+</sup>-doped substrate side contact.  $V_g$  pulse parameters include base/peak voltage  $V_{gb}/V_{gp}$  and rising/falling time  $t_r/t_f$ .

In Fig. 2, an LT TFT transfer curve at a drain voltage ( $V_d$ ) of 0.1 V is plotted in semi-log and linear scales.  $V_{fb} = 0$  V is estimated as the  $V_g$  bias of the minimum drain current ( $I_d$ ) [12].  $V_{th} = 10$  V is extracted as the intercept of linear extrapolation of the transfer curve. According to the MOSFET CP model [1]–[3],  $I_{cp}$  should be obtained when  $V_g$  pulses span the hatched transition region between  $V_{fb}$  and  $V_{th}$ . For example, if  $I_{cp}$  is measured by using  $V_g$  pulses with fixed amplitude  $V_{ph} = 22$  V and increasing  $V_{gb}$  (e.g., pulses I to V in Fig. 2),  $I_{cp}$  arises for the  $V_g$  pulses between pulses II ( $V_{gp} = V_{th}$ ) and IV ( $V_{gb} = V_{fb}$ ). When the entire  $V_g$  pulse is within the accumulation or strong inversion region, such as pulse I ( $V_{gp} = V_{fb}$ ) or V ( $V_{gb} = V_{th}$ ), no  $I_{cp}$  arises. Thus, an ideal Elliot curve is cap shaped, where  $V_{fb}$  and  $V_{th}$  are critical onset  $V_g$ 's of the constant  $I_{cp}$  [1]–[3]. The dotted line is a measured Elliot curve from the LT TFT by using optimized  $V_g$  pulses with  $V_{ph} = 22$  V and a large enough  $t_r/t_f$  of 1 ms to minimize the geometric effect [10]. However, unlike the MOSFET model, the onset  $V_g$ 's in TFTs are apparently irrelevant to  $V_{fb}$  and  $V_{th}$ , and the edges of the Elliot curve are not steep at all. Therefore, in poly-Si TFTs, it is more reasonable that each edge corresponds to two different  $V_g$  values at the start and end points, respectively.

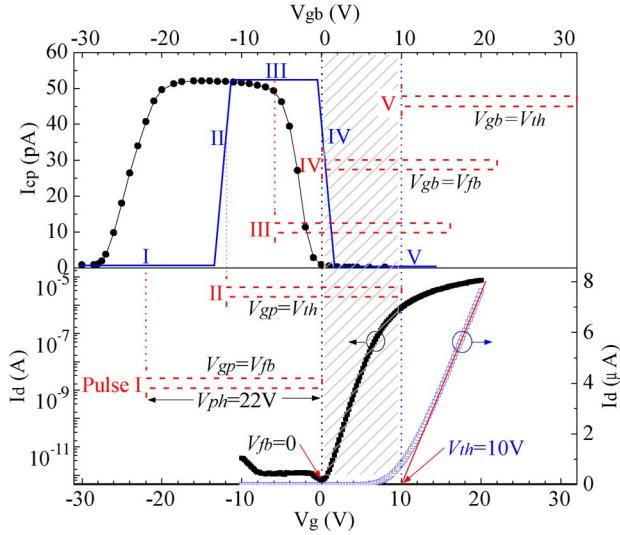


Fig. 2. LT TFT transfer curve at  $V_d = 0.1$  V is plotted in linear and semi-log scales, where  $V_{fb}$  and  $V_{th}$  are extracted. As indicated by the pulses I to V, the MOSFET CP model of the (blue line) Elliot curve corresponds to extracted  $V_{fb}$  and  $V_{th}$  and is different from the (black solid line) experimental curve of the LT TFTs measured with a  $V_{ph}$  of 22 V, a pulse period of 10 ms, a pulse duty ratio of 50%, and a  $t_r/t_f$  of 1 ms.

### III. OBSERVATION OF THE NEW CORRESPONDENCE

There is a key difference between poly-Si TFTs and MOSFETs. In MOSFETs,  $V_{th}$  is the onset of the channel strong inversion, while in poly-Si TFTs, at  $V_g = V_{th}$ , not only are the channel grains in strong inversion but also the grain boundary potential barriers are sufficiently suppressed for the carrier to flow over [13]. Therefore,  $V_{tn}$  is defined to denote the required  $V_g$  for strong inversion in n-channel TFTs, where electron concentration ( $n_e$ ) becomes reasonably high [13]. In Fig. 3, the gate-to-channel capacitance ( $C_{gc,e}$ ) of an n-channel LT TFT is measured against  $V_g$ . From the  $CV$  curve, the sheet density of the inversion electron ( $Q_e$ ) versus  $V_g$  is obtained.  $V_{tn}$  is extracted from the intercept of its linear extrapolation [13]. To reasonably compare the  $CV$  and CP tests, the same traps should be involved because only fast traps can respond to the measurement signal at a certain  $f$  (or  $t_r/t_f$ ) for the  $CV$  (or CP) test due to varied trap emission time [14]. Therefore, a proper  $f$  is determined as 30 kHz (or 10 kHz) in LT (or HT) TFTs [14]. The obtained  $V_{tn}$  of 3.2 V is much smaller than  $V_{th}$ , although, in MOSFETs, they are the same. Similarly,  $V_{tp}$  is defined as the required  $V_g$  where the hole density ( $n_h$ ) becomes reasonably high. In MOSFETs,  $V_{tp}$  equals  $V_{fb}$  since the substrate is usually moderately p-doped. In LT TFTs,  $V_{tp} = -6.6$  V is extracted by measuring the  $CV$  between the gate and the p<sup>+</sup>-doped substrate contact (see Fig. 3). It largely differs from  $V_{fb}$  too. With  $V_{tn}$  and  $V_{tp}$  extracted, three  $V_g$  regions can be defined: accumulation ( $V_g < V_{tp}$ ), inversion ( $V_g > V_{tn}$ ), and transition ( $V_{tp} < V_g < V_{tn}$ ) regions. Comparing the experimental Elliot curve with  $V_{tp}$  and  $V_{tn}$  in Fig. 3, a constant  $I_{cp}$  is obtained when  $V_g$  pulses span the hatched transition region. Moreover, when the entire pulse is within the accumulation or inversion region,  $I_{cp}$  decays to a minimum level as shown by the log-scale plot. A new correspondence for the Elliot curve is observed. The start and end points of the rising (or falling) edge of the Elliot curves

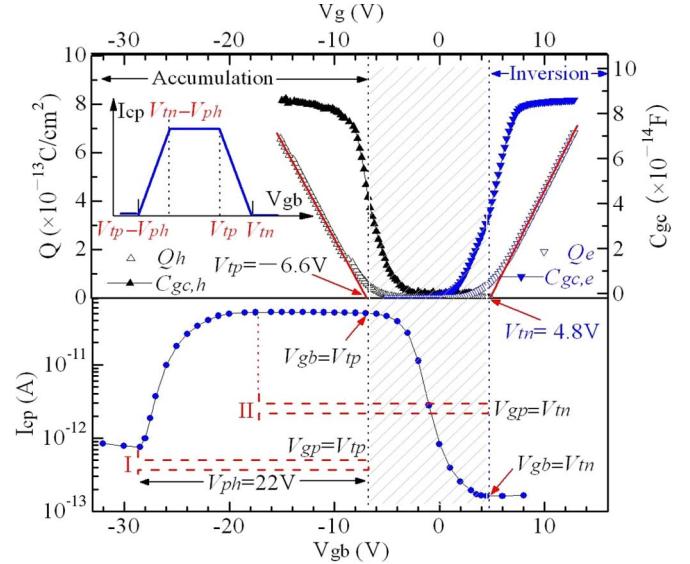


Fig. 3. LT TFT  $CV$  curves at  $f = 30$  kHz are measured between gate and drain or substrate and used to calculate  $Q - V_g$  curves from which  $V_{tn}$  and  $V_{tp}$  are extracted and correspond to the experimental Elliot curve of Fig. 2 replotted in the semi-log scale, which suggests a new correspondence between the Elliot curve and TFT key parameters in the inset.

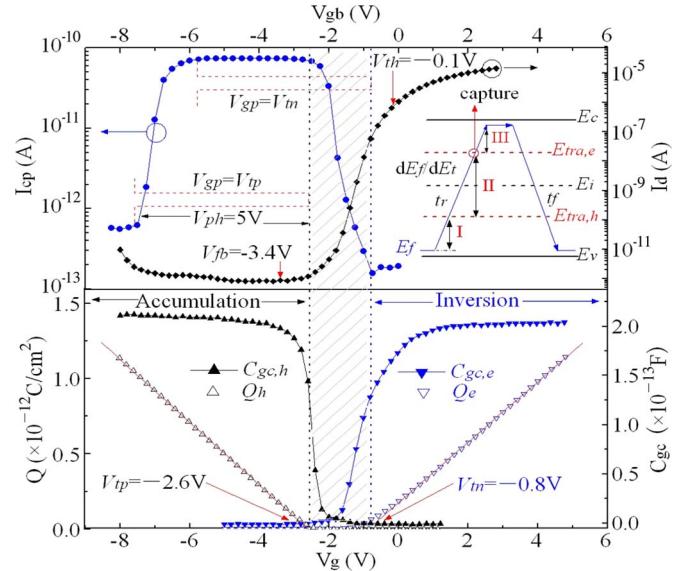


Fig. 4. HT TFT Elliot curve is measured with a  $V_{ph}$  of 5 V, a pulse period of 10 ms, a pulse duty ratio of 50%, and a  $t_r/t_f$  of 1 ms. Its onset  $V_g$ 's are observed to be  $V_{tp}$  and  $V_{tn}$  extracted from  $CV$  curves at  $f = 10$  kHz, rather than  $V_{fb}$  and  $V_{th}$  obtained from transfer curves at  $V_d = 0.1$  V.

in poly-Si TFTs should correspond to  $V_{gb} = V_{tp} - V_{ph}$  and  $V_{tn} - V_{ph}$  (or  $V_{gb} = V_{tp}$  and  $V_{tn}$ ), while the onset  $V_g$ 's of the constant  $I_{cp}$  are  $V_{tp}$  and  $V_{tn}$ . In Fig. 4, the same correspondence is observed in HT TFTs, although the discrepancy between  $V_{fb}/V_{th}$  and  $V_{tp}/V_{tn}$  in HT TFTs is notably smaller than that in LT TFTs since the fabrication process strongly affects the TFT quality and HT recrystallization produces much better poly-Si crystallinity. The same correspondence is also observed at other  $f$ 's for the  $CV$  and respective  $t_r/t_f$ 's for the CP test.

Comparing Elliot curves in MOSFETs and TFTs, the onset  $V_g$ 's of the constant  $I_{cp}$  largely differ. It can be understood from the CP model [1]–[3]. In the inset in Fig. 4, during  $t_r$ ,

surface potential ( $E_f$ ) is swept at a certain rate,  $dE_f/dt$  ( $\dot{E}_f$ ). In order to keep the trap occupation in equilibrium with the  $E_f$  sweep, holes trapped in donorlike traps will be emitted to the valence band ( $E_v$ ) at a rate

$$(\dot{E}_t)_h = kT v_{th} \sigma n_h \quad (1)$$

where  $E_t$ ,  $k$ ,  $T$ ,  $\sigma$ , and  $v_{th}$  are the trap quasi-Fermi level, Boltzmann constant, temperature, capture cross section, and thermal velocity, respectively [3]. The sweeping  $E_f$  drives TFTs from accumulation to inversion.  $n_h$  is initially high enough; thus,  $(\dot{E}_t)_h = \dot{E}_f$  so that the hole emission is in a steady state (region I). Subsequently, with  $n_h$  reduced and  $(\dot{E}_t)_h < \dot{E}_f$ , nonsteady-state emission occurs (region II). It continues until  $n_e$  becomes high enough so that  $(\dot{E}_t)_e > \dot{E}_f$  and the steady-state electron capture occurs (region III). Transition trap levels  $E_{tra,h}$  and  $E_{tra,e}$  are defined to separate regions I, II, and III by equating  $\dot{E}_f$  with  $(\dot{E}_t)_h$  or  $(\dot{E}_t)_e$  [1]–[3]. The remaining holes between the two levels after the nonsteady-state emission will be recombined with the captured electrons from the conduction band ( $E_c$ ) and contribute to  $I_{cp}$ . A similar process occurs also during  $t_f$ . Thus, the onsets of  $I_{cp}$  are  $V_g$  positions corresponding to  $E_{tra,h}$  and  $E_{tra,e}$ , respectively [1]–[3]. According to (1), obviously, only when  $n_e$  or  $n_h$  becomes reasonably high can  $(\dot{E}_t)_e$  or  $(\dot{E}_t)_h$  meet  $\dot{E}_f$  [3]. That is why the onset  $V_g$ 's of the constant  $I_{cp}$  should be  $V_{tp}$  and  $V_{tn}$ . They are more fundamental and reduce to  $V_{fb}$  and  $V_{th}$  in MOSFETs. Both experimental evidences and theoretical analysis demonstrate the applicability of  $V_{tp}$  and  $V_{tn}$  as onset  $V_g$ 's of the constant  $I_{cp}$ . Thus,  $D_t$  extraction equations for TFTs [10] should be modified by revising the onset  $V_g$ 's as  $V_{tp}$  and  $V_{tn}$ . Since the analysis is based on general CP models [1]–[3], we expect that such a correspondence should be also applicable to other field-effect devices, such as SiC MOSFETs [8].

On the other hand, the transition edges of TFT Elliot curves are much broader than those in MOSFETs. It may derive from two aspects. First, the poly-Si TFT channel consists of many grains. Their  $V_{tp}$  and  $V_{tn}$  depend on the grain size and  $D_t$  and vary in several volts [15]. Generally, the mentioned device  $V_{tp}$  (or  $V_{tn}$ ) is associated with the accumulation (or inversion) of the entire channel, i.e., close to the maximum  $V_{tp}$  (or  $V_{tn}$ ) among all grains. Each grain provides an “Elliot curve,” the sum of which is the measured overall Elliot curve. Thus, transition edges may derive from those grains with smaller  $V_{tp}$  and  $V_{tn}$ , while the constant  $I_{cp}$  originates from all grains. Hence, the onset  $V_g$ 's are device  $V_{tp}$  and  $V_{tn}$ . Therefore, the large variation of  $V_{tp}$  and  $V_{tn}$  among all grains can contribute to the broad transition edges of the TFT Elliot curve. Second, the effects that broaden MOSFET transition edges [1] may still work in TFTs, e.g., the lateral variation of  $V_{th}$  and  $V_{fb}$  near the source and drain junctions [1]. Both aspects should contribute to the gradual transition edges of the TFT Elliot curves.

#### IV. CONCLUSION

Unlike in MOSFETs, the onset  $V_g$ 's of the constant  $I_{cp}$  in poly-Si TFTs are not the  $V_{fb}$  and  $V_{th}$  derived from the transfer curve but are the  $V_{tp}$  and  $V_{tn}$  extracted from the  $CV$  curve. They are consistent with the CP model [3] and reduce to  $V_{fb}$  and  $V_{th}$  in MOSFETs. Moreover, the variation of  $V_{tp}$  and  $V_{tn}$  among channel grains and the effects broadening MOSFET transition edges [1] should contribute to the broad transition edges of the TFT Elliot curves.

#### REFERENCES

- [1] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, “A reliable approach to charge-pumping measurements in MOS transistors,” *IEEE Trans. Electron Devices*, vol. ED-31, no. 31, pp. 42–53, Jan. 1984.
- [2] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, “Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation,” *IEEE Trans. Electron Devices*, vol. 36, no. 7, pp. 1318–1335, Jul. 1989.
- [3] D. Bauza, “A general and reliable model for charge pumping—Part I: Model and basic charge-pumping mechanisms,” *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 70–77, Jan. 2009.
- [4] N. S. Saks, S. Batra, and M. Manning, “Charge pumping in thin film transistors,” *Microelectron. Eng.*, vol. 28, no. 1–4, pp. 379–382, Jun. 1995.
- [5] M. Koyanagi, I. W. Wu, A. G. Lewis, M. Fuse, and R. Bruce, “Evaluation of polycrystalline silicon thin film transistors with the charge pumping technique,” in *IEDM Tech. Dig.*, 1990, pp. 863–866.
- [6] C. Y. Chen, M. W. Ma, W. C. Chen, H. Y. Lin, K. L. Yeh, S. D. Wang, and T. F. Lei, “Analysis of negative bias temperature instability in body-tied low-temperature polycrystalline silicon thin-film transistors,” *IEEE Electron Device Lett.*, vol. 29, no. 2, pp. 165–167, Feb. 2008.
- [7] T. Yoshida, Y. Ebiko, M. Takei, N. Sasaki, and T. Tsuchiya, “Grain-boundary related hot carrier degradation mechanism in low-temperature polycrystalline silicon thin-film transistors,” *Jpn. J. Appl. Phys.*, vol. 42, no. 4B, pp. 1999–2003, 2003.
- [8] D. Okamoto, H. Yano, T. Hatayama, Y. Uraoka, and T. Fuyuki, “Analysis of anomalous charge pumping characteristics on 4H-SiC MOSFETs,” *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2013–2020, Aug. 2008.
- [9] G. Van den Bosch, G. Groeseneken, and H. E. Maes, “On the geometric component of charge pumping current in MOSFETs,” *IEEE Electron Device Lett.*, vol. 14, no. 3, pp. 107–109, Mar. 1993.
- [10] L. Lu, M. Wang, and M. Wong, “Geometric effect elimination and reliable trap state density extraction in charge pumping of polysilicon thin-film transistors,” *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 517–519, May 2009.
- [11] B. Zhang, Z. Meng, S. Zhao, M. Wong, and H. S. Kwok, “Polysilicon thin film-transistors with uniform and reliable performance using solution-based metal-induced crystallization,” *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp. 1244–1248, May 2007.
- [12] C. Y. Chen, J. W. Lee, S. D. Wang, M. S. Shieh, P. H. Lee, W. C. Chen, H. Y. Lin, K. L. Yeh, and T. F. Lei, “Negative bias temperature instability in low-temperature polycrystalline silicon thin-film transistors,” *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2993–3000, Dec. 2006.
- [13] H. Hao, M. Wang, B. Zhang, X. Shi, and M. Wong, “A comprehensive analytical on-current model for polycrystalline silicon thin film transistors based on effective channel mobility,” *J. Appl. Phys.*, vol. 103, no. 9, pp. 094513-1–094513-10, May 2008.
- [14] M. D. Jacunski, M. S. Shur, and M. Hack, “Threshold voltage, field effect mobility, and gate-to-channel capacitance in polysilicon TFTs,” *IEEE Trans. Electron Devices*, vol. 43, no. 9, pp. 1433–1440, Sep. 1996.
- [15] C. A. Dimitriadi and D. H. Tassis, “On the threshold voltage and channel conductance of polycrystalline silicon thin-film transistors,” *J. Appl. Phys.*, vol. 79, no. 8, pp. 4431–4437, Apr. 1996.