A Comparative Study on the Effects of Annealing on the Characteristics of Zinc Oxide Thin-Film Transistors With Gate-Stacks of Different Gas-Permeability

Lei Lu, Jiapeng Li, and Man Wong, *Senior Member, IEEE*

***Abstract*— The effects of different thermal processing on the characteristics of zinc oxide (ZnO) thin-film transistors (TFTs) with either gas-permeable or sealed gate-stack were studied and compared. The characteristics of a TFT heat-treated in a nonoxidizing ambience or under a sealed configuration degraded with increasing annealing temperature, though the former offered a comparatively wider process margin. On the other hand, the oxidization of the channel region of a TFT allowed by a gas-permeable gate-stack resulted in significant improvement in the transistor characteristics, e.g., eliminating the hysteresis and increasing the field-effect mobility to a relatively high value of 55 cm^2/Vs. The difference in behavior is attributed to the annealing-dependent generation and annihilation of defects in ZnO under different coverage configurations, and suggests a general guideline on the thermal processing of ZnO TFTs.**

***Index Terms*— Zinc oxide, thin-film transistor, annealing, oxygen, nitrogen, permeable, gate-stack, defect.**

I. Introduction

WITH their relatively low process temperature, high field-effect mobility, low leakage current and high transparency, thin-film transistors (TFTs) based on zinc oxide (ZnO) and its variants are being investigated as promising alternatives to low-temperature polycrystalline silicon TFTs for the construction of the next-generation flat-panel displays [1].

The characteristics of a TFT are known to depend on the thermal processes to which a TFT is subjected during its fabrication [2], [3]. This is particularly true for a TFT based on a metal-oxide semiconductor, since its properties have been shown [4] to sensitively depend on the permeability of the cover layer during a heat-treatment. In practice, the channel region of a TFT is covered by one or a combination of a gate-stack [3], [5] or a passivation layer [6]. Presently reported are the results of a comparative study on the effects of the interplay between the permeability of the coverage configuration and the annealing conditions on the characteristics of a ZnO TFT. The observed difference is correlated with the annihilation and generation of donor-like and grain-boundary defects in the channel region of the TFT.

Manuscript received May 6, 2014; revised May 20, 2014; accepted May 23, 2014. Date of publication June 13, 2014; date of current version July 22, 2014. This work was supported by the Partner State Key Laboratory on Advanced Displays and Optoelectronics Technologies under Grant ITC-PSKL12EG02. The review of this letter was arranged by Editor A. Chin.

The authors are with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong (e-mail: luleiece@ust.hk).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2014.2326960

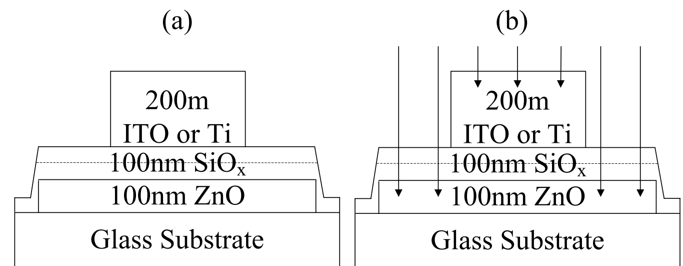

Fig. 1. The schematic cross-sections of a TFT during (a) heat-treatment and (b) S/D formation.

II. Annealing Effects on the Transistor Characteristics

The schematic cross-sections of a ZnO TFT with phosphorus-doped source and drain (S/D) regions [4] are shown in Figure 1. 100 nm thick ZnO was room-temperature sputtered on a Corning Inc. Eagle-2000 glass in a 13.56 MHz radio frequency magnetron sputtering machine with an ambience of 10% oxygen (O_2) and 90% argon (Ar). The 100nm thick gate dielectric, made of gas-permeable silicon oxide (SiO_x), was deposited at 300 °C in a plasma-enhanced chemical vapor deposition (PECVD) reactor. The 200 nm thick gate electrode, made of either gas-permeable indium-tin oxide (ITO) or gas-impermeable titanium (Ti), was room-temperature sputtered and patterned using a lift-off process. The resulting structures were then annealed in nitrogen (N_2) or O_2 (Fig. 1a). With the gate electrode as a mask, the self-aligned doping of the S/D regions was achieved using phosphorus ion implantation (Fig. 1b). Without any further heat-treatment, a reasonably low resistivity of ~10 mΩ·cm was obtained in the S/D regions after the SiO_x in those regions were removed using a plasma etch chemistry based on sulfur hexafluoride.

The drain current (I_d) versus the gate voltage (V_g) transfer characteristics of the TFTs were measured at a drain voltage

0741-3106 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

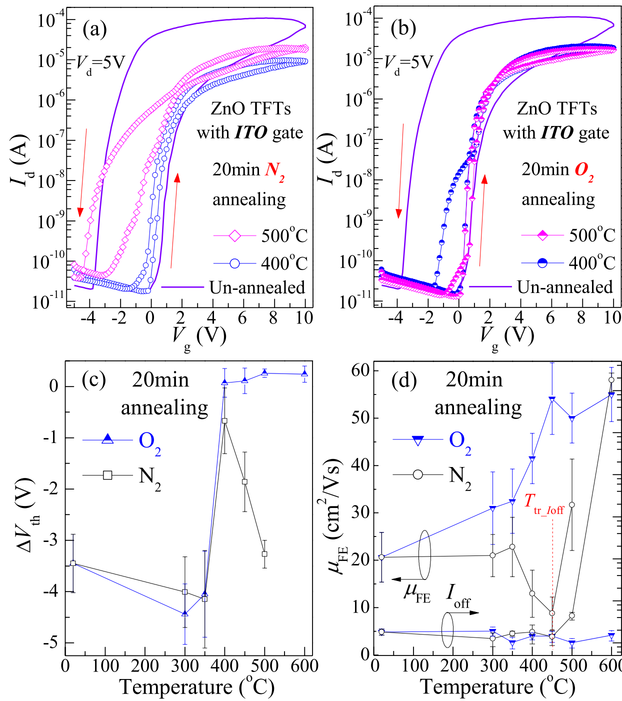

Fig. 2. The transfer characteristics of the TFTs with ITO gate (width/length = 30/16 μm) subjected to 20-minute isochronal anneals in (a) N_2 and (b) O_2. The temperature-dependence of (c) ΔV_{th} and (d) μ_{FE} and I_{off} of the corresponding TFTs.

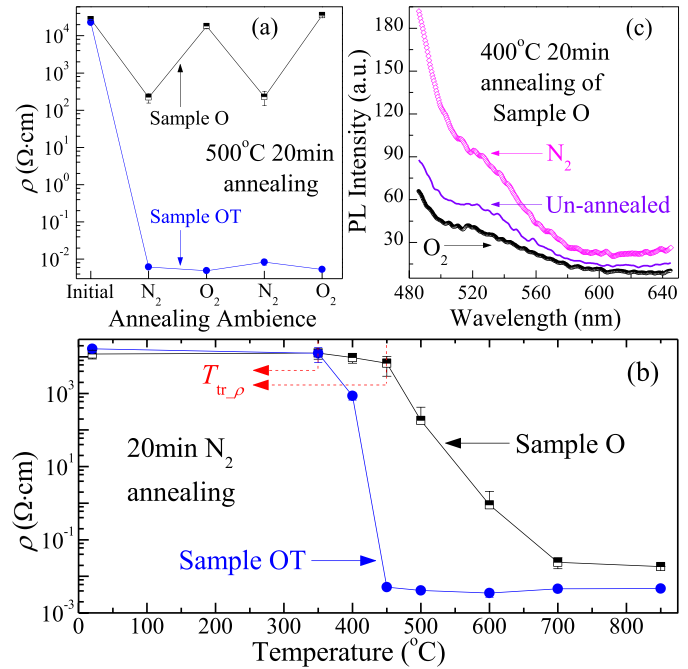

Fig. 3. The (a) ambience- and (b) temperature-dependence of the ρ for Samples O and OT subjected to 20-minute isochronal anneals at 500 °C. (c) The ambience-dependence of the PL spectra of Sample O subjected to 20-minute isochronal anneals at 400 °C in N_2 or O_2.

(V_d) of 5V under a cyclic V_g sweep. Shown in Figures 2a and 2b are those of the TFTs with gas-permeable gate-stacks heat-treated in N_2 and O_2. Anti-clockwise hysteresis is clearly visible. The linearly extrapolated threshold voltage (V_{th}) was extracted and the difference (ΔV_{th}) obtained after a cyclic sweep is used to parameterize the hysteresis (Fig. 2c). Severe hysteresis was exhibited by an un-annealed TFT, with a $\Delta V_{th} \sim -4$V. $|\Delta V_{th}|$ stayed relatively unchanged for an annealing temperature below 400 °C, but decreased significantly upon reaching 400 °C. Beyond this temperature, the temperature-dependence of the $|\Delta V_{th}|$ diverged, with the hysteresis eliminated for a TFT annealed in O_2, but increased again for one annealed in N_2.

The initial hysteresis in ZnO TFT has been attributed to the presence of H- or OH-induced electric dipoles [7], [8] located near the channel/gate dielectric interface [7]. Such species are also known to passivate interface states and supply carriers [9], resulting in an increase in the on-current. Upon annealing at a moderate temperature of 400 °C, the species were driven out of the TFT [10], leading to reduced hysteresis and on-current. For annealing beyond 400 °C in O_2, the hysteresis was completely eliminated for a TFT with a gas-permeable gate-stack. However, for annealing beyond 400 °C in N_2, the generation of defects in the ZnO channel [4] replenished the depleted dipoles – resulting in a subsequent increase in $|\Delta V_{th}|$.

The dependence of the leakage current in the off-state (I_{off}), defined as the lowest I_d in the transfer characteristics, on the annealing temperature is displayed in Figure 2d. For a TFT annealed in N_2, a steep rise in the I_{off} was observed beyond a transition temperature (T_{tr_Ioff}) of 450 °C, as has been reported [4] previously. On the other hand, a low I_{off} was consistently maintained for a TFT annealed in O_2, even up to a high temperature of 600 °C. The ambience-dependence of I_{off} is consistent with that of the resistivity (ρ) of ZnO capped with a gas-permeable SiO_x cover (Sample O) and subjected to 20-minute isochronal anneals in N_2 or O_2. The ρ was observed to change with the cyclic change of the ambience (Fig. 3a) and has been attributed to the respective generation or annihilation of donor-like defects [4] when annealed in N_2 or O_2. The temperature-dependence of ρ after 20-minute isochronal anneals in N_2 is shown in Figure 3b, exhibiting a transition to a low ρ at a characteristic temperature T_{tr_ρ}. The attribution of the change in I_{off} to the change in the residual ρ of the channel is consistent with the observation of $T_{tr_Ioff} \sim T_{tr_\rho}$.

The dependence of the field-effect mobility (μ_{FE}), extracted from the maximum of $\partial I_d^{0.5}/\partial V_g$, on the annealing temperature is also displayed in Figure 2d. For a TFT annealed in N_2, the μ_{FE} initially decreased as the temperature was raised beyond 350 °C and approached T_{tr_Ioff} – reflecting an increased hindrance against carrier transport. For a polycrystalline thin film, this most plausibly derived from an increase in the height of the grain-boundary potential barriers which was in turn induced by the generation of grain boundary traps [11]. Beyond T_{tr_Ioff}, the μ_{FE} increased with temperature. This behavior could be attributed to the generation of donor-like defects that resulted in an increase in the population of carriers energetic enough to overcome the barriers [12]. For a TFT annealed in O_2, the μ_{FE} increased rather than decreased with increasing heat-treatment temperature, eventually saturating at a relatively high value of 55 cm^2/Vs. This is consistent with the annihilation of defects [4], including those in the grain boundaries, in the channel of a TFT with a gas-permeable

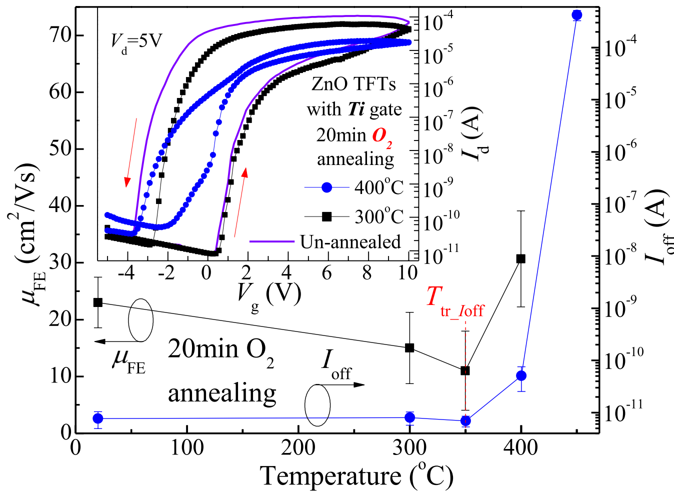

Fig. 4. The temperature-dependences of ΔV_{th} and I_{off} of the TFTs with Ti gate (width/length = 30/16 μm) subjected to 20-minute isochronal anneals in O_2. Shown in the inset are the transfer characteristics of the corresponding TFTs.

gate-stack. The population of defects in ZnO has been studied [4] using photoluminescence (PL) and is found to be consistent with the different PL spectral intensities of Sample O (Fig. 3c), subjected to heat-treatment in N_2 and O_2.

When ZnO was sealed with a gas-impermeable SiO_x/Ti double-layer (Sample OT), the exchange of the oxygen-containing species between the channel and the ambience was prohibited. Consequently, defect-annihilation did not occur even when annealed in an O_2 ambience and the ρ of Sample OT decreased to the same low value (Fig. 3a), independent of the annealing ambience. With the ITO replaced by Ti in a TFT, the gate-stack also became gas-impermeable. The temperature-dependence of the characteristics of the resulting TFT is expected to be similar to that of a TFT with a gas-permeable gate-stack annealed in N_2, due to the defect generation [4]. This is indeed verified with the data presented in Figure 4, albeit with a lower T_{tr_Ioff} that is consistent with the lower T_{tr_ρ} of Sample OT shown in Figure 3b.

III. Conclusion

The characteristics of a top-gated ZnO thin-film transistor are found to depend sensitively on the interplay between the gas-permeability of the gate-stack and the conditions of the last heat-treatment: those of a TFT subjected to an oxygen-deficient heat-treatment, either in a non-oxidizing ambience or under a sealed configuration, degraded when the temperature exceeded a certain transition temperature; Negligible hysteresis, higher field-effect mobility and lower leakage current would be obtained if the TFT were heat-treated in an oxidizing ambience, thus requiring a gas-permeable cover if the channel region was no longer exposed. Such difference in behavior is attributed to the generation and annihilation of defects in the channel region of a TFT.

References

[1] E. Fortunato, P. Barquinha, and R. Martins, “Oxide semiconductor thin-film transistors: A review of recent advances,” *Adv. Mater.*, vol. 24, no. 22, pp. 2945–2986, Jun. 2012.

[2] L. J. Brillson and Y. Lu, “ZnO Schottky barriers and ohmic contacts,” *J. Appl. Phys.*, vol. 109, no. 12, p. 121301, Jun. 2011.

[3] Z. Ye, L. Lu, and M. Wong, “Zinc-oxide thin-film transistor with self-aligned source/drain regions doped with implanted boron for enhanced thermal stability,” *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 393–399, Feb. 2012.

[4] L. Lu and M. Wong, “The resistivity of zinc oxide under different annealing configurations and its impact on the leakage characteristics of zinc oxide thin-film transistors,” *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1077–1084, Apr. 2014.

[5] T. Hirao *et al.*, “Novel top-gate zinc oxide thin-film transistors (ZnO TFTs) for AMLCDs,” *J. Soc. Inform. Display*, vol. 15, no. 1, pp. 17–22, Jan. 2007.

[6] T. Hirao *et al.*, “Bottom-gate zinc oxide thin-film transistors (ZnO TFTs) for AM-LCDs,” *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3136–3142, Nov. 2008.

[7] Z. Ye and M. Wong, “A study on the hysteresis in zinc oxide thin-film transistor with deposited silicon dioxide as the gate dielectric,” in *Proc. ICSICT*, 2012.

[8] M. Fakhri *et al.*, “Water as origin of hysteresis in zinc tin oxide thin-film transistors,” *ACS Appl. Mater. Inter.*, vol. 4, no. 9, pp. 4453–4456, Sep. 2012.

[9] K. Remashan *et al.*, “Impact of hydrogenation of ZnO TFTs by plasma-deposited silicon nitride gate dielectric,” *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2736–2743, Oct. 2008.

[10] K. Nomura *et al.*, “Defect passivation and homogenization of amorphous oxide thin-film transistor by wet O_2 annealing,” *Appl. Phys. Lett.*, vol. 93, no. 19, pp. 192107-1–192107-3, 2008.

[11] P. F. Carcia *et al.*, “Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering,” *Appl. Phys. Lett.*, vol. 82, no. 7, pp. 1117–1119, Feb. 2003.

[12] S. Bang *et al.*, “Investigation of the effects of interface carrier concentration on ZnO thin film transistors fabricated by atomic layer deposition,” *J. Phys. D, Appl. Phys.*, vol. 42, no. 23, p. 235102, Nov. 2009.