"Driving"-Stress-Induced Degradation in Polycrystalline Silicon Thin-Film Transistors and Its Suppression by a Bridged-Grain Structure

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***Abstract*— In this letter, degradation of polycrystalline silicon (poly-Si) thin-film transistors (TFTs) under "driving" stress is characterized and analyzed for the first time. Dynamic hot carrier (HC) effect, related to pulse falling time, dominates device degradation. To suppress such "driving"-stress-induced dynamic HC degradation, a bridged-grain (BG) structure is applied to the active channel of poly-Si TFTs. Due to the lateral electric field reduction at source/drain junctions, "driving"-stress-induced dynamic HC degradation is significantly improved by the BG structure. Incorporated with transient simulations, the degradation mechanism is elucidated.**

***Index Terms*— "Driving" stress, polycrystalline silicon, thin film transistor, hot carrier, bridged-grain.**

I. Introduction

POLYCRYSTALLINE silicon (poly-Si) thin-film transistor (TFT) has been used in pixel circuits in high-resolution flat-panel displays [1], such as active-matrix liquid-crystal displays (AMLCDs) and active-matrix organic light-emitting diode (AMOLED) displays. Besides the device electrical performance, the reliability of poly-Si TFTs in the pixel circuit is also an issue of concern. Compared with AMLCDs, AMOLED displays place high demands on device reliability since the decay of the lighting intensity is directly related to the degradation of TFTs [2]. The degradation of poly-Si TFTs under either DC stresses [3], [4] or AC stresses [5]–[8] has been fully investigated. Compared with those under DC stresses, the reliability tests under AC stresses have more important reference significance for pixel circuit designers. However, the AC stress conditions reported in literatures, including AC gate stress condition [5], [6] and AC drain stress condition [7], [8], are still not close to practical operation conditions applied to poly-Si TFTs in the pixel circuit of AMOLED displays. Until now, no reliability study has been performed on TFTs under the stresses that simulate practical operation conditions of pixel TFTs in AMOLED displays.

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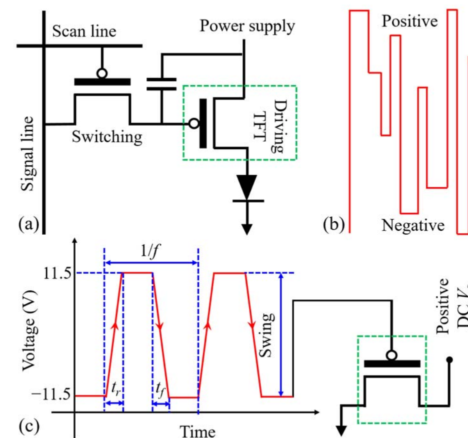

Fig. 1. (a) Schematic of 2T1C circuit of a pixel in an AMOLED display. (b) Practical voltage pattern applied to the gate electrode of the driving TFT. (c) "Driving" stress conditions for a driving TFT.

In this letter, a "driving" stress scheme, which simulates the operation conditions of a driving TFT in a pixel circuit of an AMOLED display, is proposed. Degradation of poly-Si TFTs under such "driving" stress is characterized and analyzed for the first time. It is found that the "driving"-stress-induced degradation is dominated by a dynamic hot carrier (HC) effect. Faster pulse rising time (t_r) brings larger dynamic HC degradation. By employing a bridged-grain (BG) structure in the active channel, "driving"-stress-induced degradation can be significantly reduced, which is attributed to the lateral electric field (E_x) reduction at source/drain junctions. The related degradation mechanism is proposed and discussed, incorporated with transient simulations.

II. Experimental

Shown in Fig. 1a is a schematic of a pixel circuit consisting of two TFTs and one capacitor (2T1C) in an AMOLED display. For a p-type driving TFT, the source electrode is usually connected to a positive power supply. The gate electrode suffers from irregular voltage pulses, as shown in Fig. 1b. Different gate voltage values stand for different gray levels.

To simulate such operation conditions in the driving TFT, a "driving" stress scheme, consisting of an AC gate stress and a positive DC source bias (V_s), is proposed, as shown

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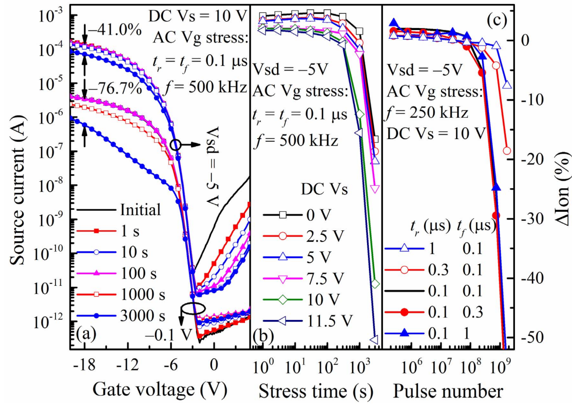

Fig. 2. (a) Time evolution of transfer characteristics under AC gate stress with DC stress V_S = 10 V in normal poly-Si TFTs. (b) I_{on} degradation dependent on stress time for AC gate stress with various DC V_S stresses in normal poly-Si TFTs. (c) I_{on} degradation dependent on pulse number for AC gate stress with various t_r and t_f in normal poly-Si TFTs. The DC stress V_S is fixed at 10 V.

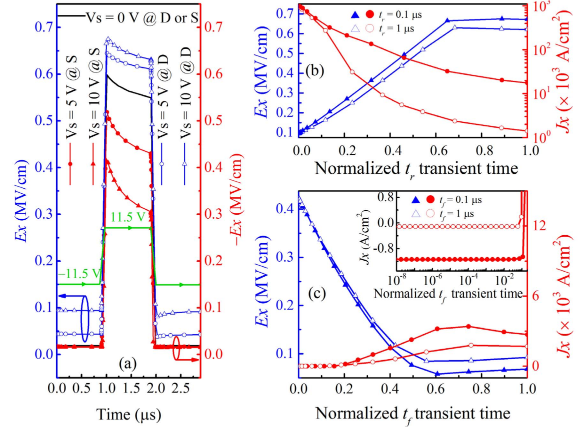

Fig. 3. (a) Dependence of extracted E_X on time in the channel at the channel/source edge and at the channel/drain edge under AC gate stress with various DC V_S stress in normal poly-Si TFTs. The green lines represent the gate pulse, and $t_r = t_f = 0.1$ μ s. (b) Dependence of the E_X and J_X on normalized t_r transient time in the channel at the drain side in normal poly-Si TFTs. (c) Dependence of the E_X and J_X on normalized t_f transient time in the channel at the drain side in normal poly-Si TFTs. The inset is the magnification of J_X at the beginning of the normalized t_f transient time.

in Fig. 1c. For the AC gate stress, the voltage pulses are set to swing from a negative value (−11.5 V) to a positive value (+11.5 V), which is regarded as the worst case for the driving TFT. Pulse parameters include pulse number, frequency (f), t_r and pulse falling time (t_f). Taking a full high definition display at 60 Hz frame rate for example, pixel designers normally set the transition time as $\sim$ μs level. Therefore, the t_r/t_f in this work is set to vary from 0.1 to 1 μs. The DC V_s varies from 0 to 11.5 V. The normal poly-Si TFTs and BG poly-Si TFTs used in this letter are of the conventional self-aligned top-gate structure. The detailed fabrication processes are presented elsewhere [4]. The channel width (W) and channel length (L) are both fixed at 10 μm for poly-Si TFTs under test. The devices were measured before and after stress by using an Agilent 4156C semiconductor parameter analyzer and the AC gate pulse was generated by Agilent 41501B. Device degradation is evaluated by a percentile change in on-state current (ΔI_{on}) with respect to its initial value (I_{on}).

III. Results and Discussion

A time evolution of the transfer characteristics under "driving" stress in the normal poly-Si TFT is shown in Fig. 2a. The "driving" stress is represented by an AC gate stress plus a DC V_s of 10 V. It can be observed that both the I_{on} and GIDL current [9] continuously decreases with the stress time whereas the subthreshold swing is hardly affected. I_{on} recovery at high V_{sd} is also observed, which can be explained by the source induced barrier lowering of the stress-induced trap potential barrier [3]. All above-mentioned degradation features accord well with typical HC degradation [3], [4], indicating such "driving"-stress-induced degradation is related to some HC mechanism.

To figure out which parameter of "driving" stress dominates the device degradation, stress tests were performed under AC gate stress with different DC V_s, f, t_r and t_f. Shown in Fig. 2b is I_{on} degradation dependent on stress time under AC gate stress with various positive DC V_s stresses in normal poly-Si TFTs. The I_{on} degradation exhibits a two-stage characteristic. In the first stage, I_{on} slightly increases with stress time, while in the second stage, I_{on} dramatically decreases with stress time. Electron trapping/injection into the gate oxide may be responsible [8] for the first-stage I_{on} increase and dynamic HC effect may dominate the second-stage I_{on} decrease. It is also observed that a larger positive DC V_s results in a smaller I_{on} increase in the first stage and a larger I_{on} decrease in the second stage. Additionally, for the DC $V_s = 0$ V, the degradation after 3000 s stress is −36.6% (V_g swing = 23 V, V_{sd} = −0.1 V). Similar stress magnitude brings −65.5% degradation in solution-based metal-induced lateral crystallization TFTs (V_g swing = 20 V) [10] and −90.0% degradation in excimer laser annealing TFTs (V_g swing = 30 V) [11]. The dramatic degradation is mainly due to dynamic HC effect [10], [11].

The degradation of normal poly-Si TFTs under "driving" stress is independent of f when plotting the degradation data against the pulse number (not shown here), indicating that the degradation is associated with pulse transition edges. Similar degradation behaviors were also observed under AC gate stress [12] and AC drain stress [8]. The effect of pulse transition edges is examined and shown in Fig .2c. Apparently, I_{on} degradation strongly depends on t_r rather than t_f. A shorter t_r brings a larger second-stage degradation, indicating the underlying dynamic HC mechanism is related to t_r rather than t_f. Noted that it is the *same* to AC-gate-stress-induced HC degradation [12] and *opposite* to AC-drain-stress-induced HC degradation [8], where more severe degradation respectively occurs at shorter t_r and at shorter t_f. In the MOSFETs [13], similar stress condition was investigated, where severe HC degradation occurs at high f, and during t_f of AC gate stress.

To analyze the "driving"-stress-induced degradation mechanism in poly-Si TFTs, a transient simulation was performed utilizing Silvaco ATLAS. Shown in Fig. 3a is the dependence of the extracted E_x on time in the channel at the channel/source edge and at the channel/drain edge under AC gate stress with various DC V_s stresses in normal poly-Si TFTs. The positive x direction is defined from the source to the drain. It can be observed that the $|E_x|$ induced by AC gate

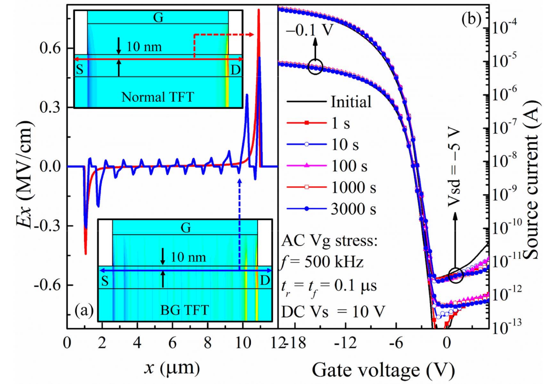

Fig. 4. (a) Extracted E_X at 10 nm below the oxide/channel interface along the drain side to the source side at the end of t_r of an AC gate pulse in a normal poly-Si TFT and a BG poly-Si TFT. The DC stress V_d is fixed at 10 V. The insets are the E_X distribution in a normal poly-Si TFT (upper) and a BG poly-Si TFT (lower). (c) Time evolution of transfer characteristics under AC gate stress with DC stress V_S = 10 V in BG poly-Si TFTs.

stress in the channel at the source side is suppressed by a higher DC V_s, while the E_x at the drain side is enlarged by a higher DC V_s. Since the HC degradation is dominated by the peak electric field [8], the dynamic HC degradation in the second stage under "driving" stress should prevail at the drain side. A higher DC V_s brings a larger E_x in the channel at the drain side, resulting in larger I_{on} degradation (Fig. 2b).

In Fig. 3b and 3c, the E_x and lateral current density (J_x) are plotted against the normalized transient time at the channel/drain edge. The positive DC V_s is fixed at 10 V. In Fig. 3b, within the t_r transition, E_x curves for different t_r increase rapidly to a high field while J_x decreases slowly. Carriers will be exposed to the high E_x and become HCs. A shorter t_r brings larger E_x and J_x, resulting in large I_{on} degradation in the second stage (Fig. 2c). In the t_f transition, as shown in Fig. 3c, E_x decreases with time. At the beginning of t_f, although the E_x is high, the J_x moves in the opposite direction to E_x, as shown in the inset of Fig. 3c. It cannot be a drift current under the E_x. No HCs will be generated. When t_f continues, the J_x begins to follow the direction of E_x. However, at this time the E_x is too low to accelerate carriers to become HCs. Therefore, dynamic HC degradation in the second stage under "driving" stress is independent of t_f (Fig. 2c).

To clarify the underlying degradation mechanism in the second stage, the non-equilibrium junction degradation model [8], is employed and developed. For the "driving" stress consisting of a AC gate stress and a positive DC V_s, at the very beginning of t_r (−11.5 V to 11.5 V), the source junction is forward biased while the drain junction is reversely biased. The $|E_x|$ in the channel at the drain side is larger than that at source side. Higher positive DC V_s makes the source junction more forward biased and the drain junction more reversely biased, resulting in the suppressed $|E_x|$ at source side and enlarged $|E_x|$ at drain side, as shown in Fig. 3a. As t_r continues, forward biased source junction become reversely biased while the reversely biased drain junction become more and more reversely biased. The depletion region in the channel around both junctions need to extend by emitting trap-related carriers. For the drain junction, since the depletion region in the channel already exists and the electric field is high, emitted carriers can gain enough energy to become HCs. For the source junction, only later emitted carriers from the deep trap states are exposed to a high E_x across the depletion region and can gain enough energy to become HCs. This explains why the HC degradation prevails at drain junction under "driving" stress. For t_f transient, the extended depletion region into the channel should shrink back. Ionized traps during the t_r transient are neutralized from the outer edge of the depletion region via carrier recombination. E_x therein is very low and no HCs can be generated. Thus, the degradation is independent of t_f.

The E_x at the channel/source junction and channel/drain junction is concluded to be a dominant factor inducing dynamic HC degradation under "driving" stress. If E_x can be reduced, the dynamic HC degradation would be alleviated. The BG structure can reduce the E_x at junctions by a sharing of the E_x across the multiple p-n junctions inherent in the channel [4], [14]. The "driving"-stress-induced HC degradation may be improved in BG poly-Si TFTs. The simulation of E_x distribution in a normal poly-Si TFT (upper) and a BG poly-Si TFT (lower) at the end of t_r of an AC gate pulse were performed, as shown in insets of Fig. 4a. The $t_r = 0.1\ \mu$s and DC $V_s = 10$ V. It can be observed that the intensity of E_x at channel/source junction and channel/drain junction in BG poly-Si TFTs is weakened by the sharing of the field across multiple reverse biased junctions. To be clearer, the E_x at 10 nm below the oxide/channel interface along the source side to the drain side in the normal poly-Si TFT (red line) and the BG poly-Si TFT (blue line) is extracted. The peak value of E_x at both the channel/source junction and channel/drain junction is reduced via employing a BG structure in the active channel, indicating a better dynamic HC reliability in BG poly-Si TFTs. Reliability test in BG poly-Si TFTs under the same "driving" stress was then performed, as shown in Fig. 4b. Compared with the normal poly-Si TFTs (Fig. 2a), the transfer curve of BG poly-Si TFTs keeps almost the same after "driving" stress. Extracted from the transfer curve degradation of the normal poly-Si TFT (Fig. 2a) and BG poly-Si TFT (Fig. 4b) after 3000 s "driving" stress, the I_{on} degradation of the normal poly-Si TFT at $V_{sd} = -0.1$ and −5 V are respectively −76.7% and −41.0%, while the I_{on} degradation of the BG poly-Si TFTs are only respectively −3.6% and −1.60%. This is mainly due to a series of reversed junctions in the BG poly-Si TFTs that share the voltage drop, as depicted in Fig. 4a. The HC degradation is strongly dependent on E_x [13]. The BG poly-Si TFT will show similar substantial degradation as the normal poly-Si TFT (Fig. 2a) under AC V_g stress swinging from −14.7 V to 14.7 V (DC $V_s = 10$ V), where the peak E_x at the end of t_r in BG poly-Si TFTs is comparable to that in normal poly-Si TFTs.

IV. Conclusion

The "driving"-stress-induced degradation in poly-Si TFTs is studied for the first time. Dynamic HC effect dominates the device degradation. The non-equilibrium junction degradation model is further developed to explain the observed degradation behaviors. To suppress such dynamic HC degradation, a BG structure is applied and the BG poly-Si TFTs show excellent reliability performance under the "driving" stress.

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