Dynamic-Gate-Stress-Induced Degradation in Bridged-Grain Polycrystalline Silicon Thin-Film Transistors

Meng Zhang, Zhihe Xia, Wei Zhou, Rongsheng Chen, Man Wong, *Senior Member, IEEE*, and Hoi-Sing Kwok, *Fellow, IEEE*

***Abstract*— In this paper, degradation behaviors of bridged-grain (BG) polycrystalline silicon (poly-Si) thin-film transistors (TFTs) are systematically characterized and investigated. Device degradation exhibits a two-stage behavior, which is related to pulse falling time (t_f). A faster t_f brings a larger ON-current (I_{ON}) increase in the first stage and a larger I_{ON} decrease in the second stage. Electron trapping/injection into gate oxide and dynamic hot carrier effect are found to be responsible to I_{ON} increase in the first stage and I_{ON} decrease in the second stage, respectively. Compared with normal poly-Si TFTs, BG poly-Si TFTs show much more reliable performance under the same dynamic gate stress. The larger I_{ON} increase in the first stage in BG poly-Si TFTs is attributed to the enhanced vertical electric field in the channel near the gate oxide, while the much smaller I_{ON} decrease in the second stage is attributed to lateral electric field reduction caused by the sharing of the field across multiple reversely biased junctions inside the active channel. Incorporated with transient simulations, the degradation mechanisms for both the first stage and the second stage are elucidated. In addition, the impact of the first-stage degradation on the second-stage degradation is also clarified.**

***Index Terms*— Bridged grain (BG), dynamic gate stress, polycrystalline silicon (poly-Si), thin-film transistors (TFTs).**

I. Introduction

POLYCRYSTALLINE silicon (poly-Si) thin-film transistors (TFTs) have become one of the most promising candidates to integrate pixel elements with driver circuits to achieve the system-on-panel (SoP) applications [1], [2]. High-performance and high-reliable poly-Si TFTs are required to accomplish the above purpose. Unlike those in the pixels, TFTs in driver circuits are subjected to high-frequency (f) voltage pulses and suffer from dynamic degradation [3]. Therefore, poly-Si TFTs with superb dynamic reliability are desired. Dynamic-stress-induced degradation in poly-Si TFTs, mainly including dynamic-gate-stress-induced degradation [4]–[6] and dynamic-drain-stress-induced degradation [7]–[9], has been extensively investigated. Dynamic hot carrier (HC) effect [4]–[9], occurring during the pulse transient time, is found to be the dominant degradation mechanism in poly-Si TFTs. However, a few methods have been proposed to alleviate such dynamic-stress-induced degradation in poly-Si TFTs.

Recently, bridged-grain (BG) technology [10]–[15] has been invented and introduced to generate high-performance poly-Si TFTs. Static-stress-induced degradation in BG poly-Si TFTs has been systematically characterized in investigated [16]. Compared with normal poly-Si TFTs, BG poly-Si TFTs exhibit excellent static HC reliability, self-heating reliability, and negative bias temperature instability (NBTI). One may wonder whether BG poly-Si TFTs could also exhibit excellent reliability performance under dynamic stress.

In this paper, device degradation behaviors and mechanisms under dynamic gate stress are systematically characterized and investigated in both normal poly-Si TFTs and BG poly-Si TFTs. A two-stage degradation behavior in both normal poly-Si TFTs and BG poly-Si TFTs is observed under the dynamic gate stress. Both ON-current (I_{ON}) increase in the first stage and I_{ON} decrease in the second stage are augmented by a faster pulse falling time (t_f). Compared with normal poly-Si TFTs, BG poly-Si TFTs exhibit a larger I_{ON} increase in the first stage and a smaller I_{ON} decrease in the second stage under the same dynamic gate stress. Electron trapping/injection into the gate oxide and dynamic HC effect are confirmed to be the dominant mechanisms in the first-stage degradation and second-stage degradation, respectively. The larger I_{ON} increase in the first stage in BG poly-Si TFTs is attributed to the enhanced vertical electric field (E_y) in the channel near the gate oxide, while the smaller I_{ON} decrease in the second stage is mainly attributed to the reduced lateral electric field (E_x) in the channel at source/drain sides. Incorporated with transient simulations, both the first-stage degradation mechanism and the second-stage degradation mechanism are clarified. Moreover, the impact of first-stage degradation on the second-stage degradation is also explained.

II. Experiments

Cross-sectional schematic of the BG poly-Si TFT is shown in Fig. 1(a), and the device fabrication is described as follows. The 4-in sized silicon wafers covered with

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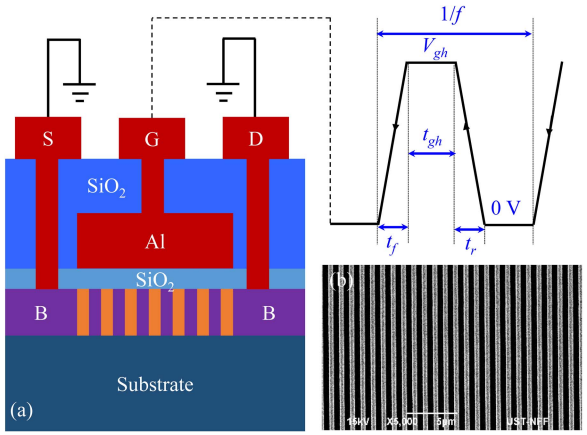

Fig. 1. (a) Cross-sectional schematic of the BG poly-Si TFT and waveforms of dynamic gate stress applied to the gate electrode with source/drain electrodes grounded. (b) SEM image of PR pattern of BG lines.

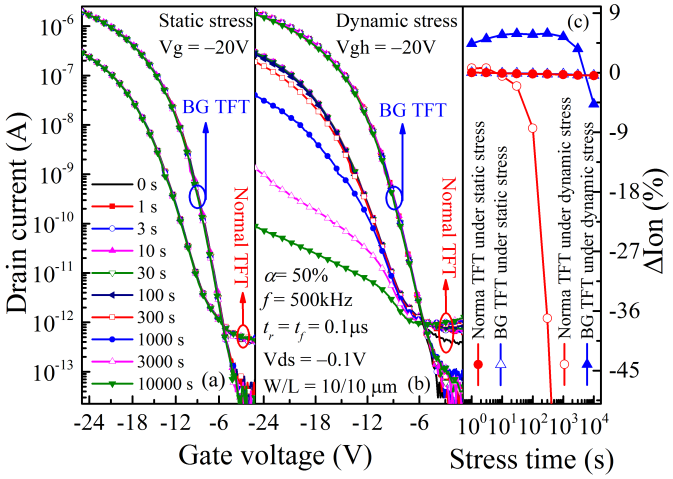

Fig. 2. Time evolution of transfer characteristics for normal poly-Si TFTs and BG poly-Si TFTs under (a) static gate stress and (b) dynamic gate stress. (c) Extracted I_{ON} degradation dependent on stress time under the static gate stress and dynamic gate stress in both normal and BG poly-Si TFTs.

500-nm-thick thermal oxide were applied as the starting substrates and 50-nm-thick amorphous silicon (a-Si) was deposited onto the substrate through low-pressure chemical vapor deposition (LPCVD) at 550 °C as the active layer. Then, 5-nm-thick nickel (Ni) was evaporated onto the surface of a-Si layer, followed by nitrogen annealing at 600 °C for 6 h to convert the a-Si film into a poly-Si film. After annealing, the wafer was treated by sulfuric acid cleaning to remove Ni. Then, 50-nm-thick low-temperature oxide (LTO) was deposited by LPCVD at 425 °C, which would serve as the sacrificial layer for BG ion implantation. Next, a layer of photoresist (PR) was spin coated and patterned into gratings with a period of 1 μm and an aspect ratio of 50%. Structures of the patterned PR captured by the scanning electron microscope (SEM) are shown in Fig. 1(b). Boron implantation with a dose of 2×10^{15} cm^{-2} was performed to the exposed areas through the gratings. After implantation, the PR and LTO sacrificial layer were removed, followed by active island patterning. Then, 70-nm-thick SiO_2 deposited by LPCVD at 425 °C was employed as gate dielectric. After gate dielectric deposition, 300-nm-thick aluminum (Al) was subsequently sputtered and patterned as gate electrodes. The source and the drain were formed by a self-aligned boron implantation at a dosage of 5×10^{15} cm^{-2}. After formation of the source/drain, a 500-nm-thick LTO layer was deposited as an isolation layer. The contact holes were defined, and 700-nm-thick Al–1% Si was subsequently sputtered and patterned as testing pads. The devices were then sintered in forming gas for 30 min at 420 °C. No further passivation was applied to these devices. For comparison, normal poly-Si TFTs were also fabricated at the same time by going through the same processes only without the BG treatment.

For poly-Si TFTs under test, the channel width (W) and length (L) are both fixed at 10 μm. As shown in Fig. 1(a), square gate pulse stress is applied to gate electrode with source/drain electrodes grounded. The gate pulse swings from 0 V to a negative peak voltage of V_{gh}. The V_{gh} value varies from -15 to -35 V. Pulse parameters include pulse duty ratio (α), f, pulse number, V_{gh}, pulse ring time (t_r), and t_f. Device degradation is evaluated by a percentile change in I_{ON} with respect to its initial value (ΔI_{ON}).

III. Results and Discussion

Transfer curve degradation behaviors under static gate stress and dynamic gate stress in both normal poly-Si TFTs and BG poly-Si TFTs are shown in Fig. 2. It can be clearly observed that the performance of unstressed BG poly-Si TFTs is much better than that of unstressed normal poly-Si TFTs in terms of smaller threshold voltage, steeper subthreshold swing, and larger I_{ON}/OFF-current ratio. By electively doping BG lines inside the active channel, grain size effect, short channel effect, and multijunction effect are beneficially exploited, resulting in excellent device electrical performance in BG poly-Si TFTs [10]–[15]. Shown in Fig. 2(a) is a time evolution of transfer characteristics for normal poly-Si TFTs and BG poly-Si TFTs under a static gate stress. The static gate stress of -20 V is applied to the gate electrode with the source/drain electrodes grounded. It can be observed that almost no degradation occurs in both normal poly-Si TFTs and BG poly-Si TFTs. The extracted I_{ON} degradation is shown in Fig. 2(c). After 10^4-s static gate stress, the I_{ON} degradation is only -0.42% in normal poly-Si TFTs and -0.44% in BG poly-Si TFTs. It can be considered that no static degradation occurs during the static gate stress of -20 V. However, under a dynamic gate stress with $V_{gh} = -20$ V, as shown in Fig. 2(b), the degradation of the normal poly-Si TFTs is significantly augmented. The I_{ON} drastically decreases with stress time. Interestingly, the transfer curve of BG poly-Si TFTs is nearly unchanged with the stress time under the same dynamic gate stress.

By examining the device degradation more carefully, the I_{ON} degradation of both normal poly-Si TFTs and BG poly-Si TFTs exhibits a two-stage degradation behavior, as shown in Fig. 2(c). The I_{ON} value first increase in the first stage and then decrease in the second stage. Similar degradation behaviors are also observed in the previous reports [9], [17]. The electron trapping/injection into gate oxide may be responsible

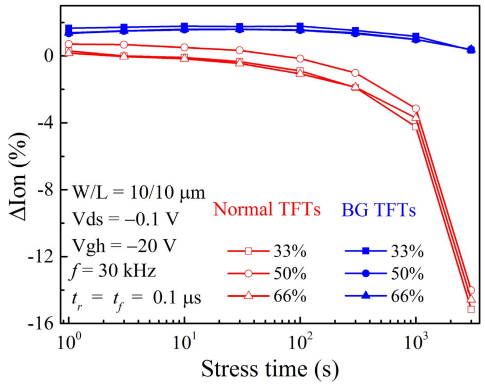

Fig. 3. I_{ON} degradation dependent on stress time under dynamic gate stresses with various αs in normal poly-Si TFTs and BG poly-Si TFTs.

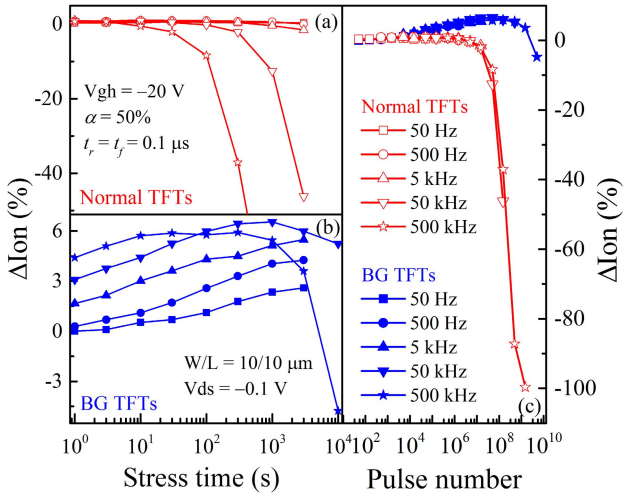

Fig. 4. I_{ON} degradation dependent on stress time under dynamic gate stresses with various fs in (a) normal poly-Si TFTs and (b) BG poly-Si TFTs. (c) I_{ON} degradation dependent on pulse number under dynamic gate stresses with various fs in normal poly-Si TFTs and BG poly-Si TFTs.

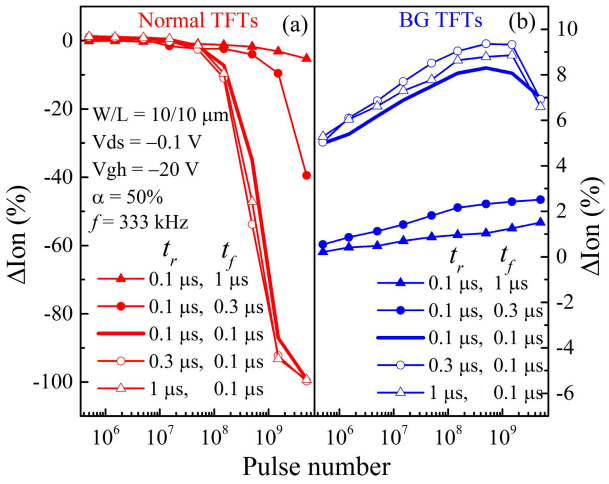

Fig. 5. I_{ON} degradation dependent on pulse number under dynamic gate stresses with various t_r and t_f in (a) normal poly-Si TFTs and (b) BG poly-Si TFTs.

for the first-stage degradation, while the dynamic HC effect may be responsible the second-stage degradation. Compared with normal poly-Si TFTs, BG poly-Si TFTs show a larger I_{ON} increase in the first stage and much smaller I_{ON} decrease in the second stage. The turnaround point in the normal poly-Si TFT appears earlier than that in the BG poly-Si TFT.

To figure out which parameter of the dynamic gate stress dominates the device degradation, stress tests are performed under dynamic gate stresses with various αs, fs, t_r, t_f, and V_{gh}s. First, device degradation under dynamic gate stresses with various αs in normal poly-Si TFTs and BG poly-Si TFTs is examined, as shown in Fig. 3. The $V_{gh} = -20$ V, $f = 30$ kHz, and $t_r = t_f = 0.1$ μs. It can be observed that for both normal poly-Si TFTs and BG poly-Si TFTs, degradation curves under dynamic gate stresses with various αs overlap each other, indicating that the degradation is independent of the duration time of V_{gh} (t_{gh}). In the other word, no static effect is involved under V_{gh} of -20 V, consistent with the results shown in Fig. 2(a). Under the same dynamic gate stress, BG poly-Si TFTs exhibit much more reliable performance in terms of a larger I_{ON} increase in the first stage and a much smaller I_{ON} decrease in the second stage.

Then, device degradation under dynamic gate stress with various fs is examined, as shown in Fig. 4. The f value varies from 50 Hz to 500 kHz. The $V_{gh} = -20$ V, $\alpha = 50\%$, and $t_r = t_f = 0.1$ μs. Shown in Fig. 4(a) is I_{ON} degradation dependent on stress time under dynamic gate stresses with various fs in normal poly-Si TFTs. It can be observed that the turnaround point appears earlier for a larger f, and the degradation in the second stage is augmented by a lager f. For BG poly-Si TFTs, as shown in Fig. 4(b), similar degradation behaviors are observed. Dynamic gate stress with a larger f brings a larger I_{ON} increase in the first stage and a larger I_{ON} decrease in the second stage. The turnaround point appears earlier for a larger f. Again, compared with normal poly-Si TFTs, BG poly-Si TFTs show a larger I_{ON} increase in the first stage and a much smaller I_{ON} decrease in the second stage under the same dynamic gate stress, and the turnaround point in BG poly-Si TFTs appears later. When plotting I_{ON} degradation curves against pulse number rather stress time, as shown in Fig. 4(c), it is found that all degradation curves under dynamic gate stress with various fs follow the same trend in both normal poly-Si TFTs (red lines) and BG poly-Si TFTs (blue lines), indicating that the degradation in both two stages is associated with the pulse transition edges.

Next, the effect of pulse transition edges is examined. Shown in Fig. 5 is pulse number-dependent I_{ON} degradation under dynamic gate stresses with various t_r and t_f values in normal poly-Si TFTs [Fig. 5(a)] and BG poly-Si TFTs [Fig. 5(b)]. The $V_{gh} = -20$ V, $\alpha = 50\%$, and $f = 333$ kHz. For both normal poly-Si TFTs and BG poly-Si TFTs, I_{ON} degradation curves overlap each other under dynamic gate stresses with various t_r and fixed t_f values, indicating that the degradation is independent of t_r. For the dynamic gate stress with various t_f values, in normal poly-Si TFTs [Fig. 5(a)], a shorter t_f brings a larger I_{ON} decrease in the second stage, and the turnaround point appears earlier for a shorter t_f. In BG poly-Si TFTs, as shown in Fig. 5(b), a shorter t_f brings a larger I_{ON} increase in the first stage, and the second-stage

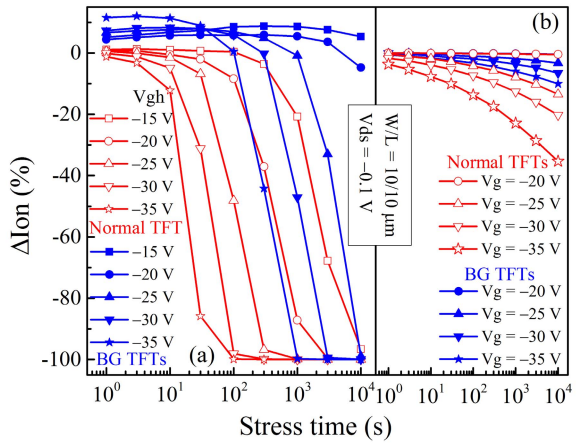

Fig. 6. I_{ON} degradation dependent on stress time (a) under dynamic gate stress with various V_{gh}s and (b) under various static gate stresses in normal poly-Si TFTs and BG poly-Si TFTs.

stage degradation is absent within the 10^4-s stress. The test results reveal that the dynamic-gate-stress-induced degradation is related to t_f rather t_r for both two stages. The BG poly-Si TFTs show much better reliable performance under the same stress condition, consistent with the above results.

Finally, degradation behaviors under dynamic gate stresses with various V_{gh}s in normal poly-Si TFTs and BG poly-Si TFTs are examined, as shown in Fig. 6(a). The $\alpha = 50\%$, $f = 500$ kHz, and $t_r = t_f = 0.1$ μs. For normal poly-Si TFTs (red lines), the turnaround point appears earlier for a larger $|V_{gh}|$, and I_{ON} degradation in the second stage is augmented by a larger $|V_{gh}|$. For BG poly-Si TFTs (blue lines), similar degradation behaviors are also observed. Compared with that in normal poly-Si TFTs, the turnaround point appears later and the degradation in the second stage is greatly alleviated in BG poly-Si TFTs. In fact, when $|V_{gh}| > 20$ V, static NBTI effect is involved to increase the second-stage degradation. Shown in Fig. 6(b) is the dependence of I_{ON} degradation on stress time for various static gate stresses in normal poly-Si TFTs and BG poly-Si TFTs. It can be observed that when $|V_g| > 20$ V, static NBTI degradation happens in both normal poly-Si TFTs and BG poly-Si TFTs. BG poly-Si TFTs exhibit more reliable static NBTI performance, mainly due to the boron–hydrogen bond formation at the interface/grain boundaries [9], [18].

To investigate the underlying mechanism of dynamic-gate-stress-induced degradation in normal poly-Si TFTs and BG poly-Si TFTs, a transient simulation was performed utilizing Silvaco ATLAS. For the I_{ON} increase in the first stage, electron trapping/injection into the gate oxide with the assistance of electric field is inferred to be responsible. The transient E_y dependent on pulse time at the channel/drain edge is first simulated in a normal poly-Si TFT and a BG poly-Si TFT, as shown in Fig. 7. The positive direction is defined from the gate electrode to the substrate. It can be observed that when the gate pulse swings from −20 to 0 V (t_f), a positive E_y is induced in both the normal poly-Si TFT and BG poly-Si TFT. With the assistance of positive E_y, electrons trapping/injection into gate oxide occurs, resulting in an I_{ON} increase in the

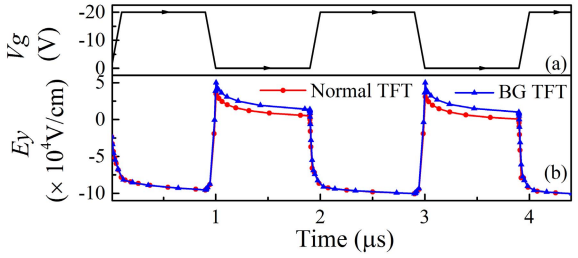

Fig. 7. (a) Dynamic gate pulse applied to the gate electrode. The $t_r = t_f = 0.1$ μs. (b) Dependence of E_y on time at the channel/drain edge near the gate oxide. The positive direction is defined from the gate electrode to the substrate.

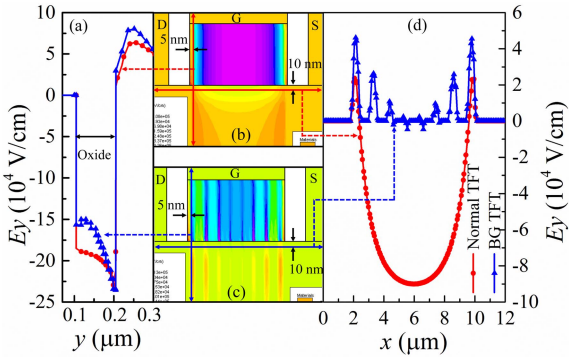

Fig. 8. (a) Extracted E_y at 5 nm close to the edge of the gate oxide along the gate electrode to the channel at the end of t_f in a normal poly-Si TFT and a BG poly-Si TFT. E_y distribution in (b) normal poly-Si TFT and (c) BG poly-Si TFT. (d) Extracted E_y at 10 nm below the oxide/channel interface along the drain side to the source side at the end of t_f in a normal poly-Si TFT and a BG poly-Si TFT.

first stage. Moreover, E_y in the BG poly-Si TFT is larger than that in the normal poly-Si TFT, which explains why the I_{ON} increase in BG poly-Si TFTs is larger than that in normal poly-Si TFTs.

To see more comprehensively and more accurately, E_y distributions at the end of t_f in a normal poly-Si TFT and a BG poly-Si TFT are simulated and shown in Fig. 8(b) and (c). It can be observed that the intensity of E_y in the channel near the gate oxide is enhanced by the BG structure. To be clearer, E_y at 5 nm close to the edge of the gate oxide along the gate electrode to the channel in the normal poly-Si TFT (red line) and BG poly-Si TFT (blue line) is extracted, as shown in Fig. 8(a). It can be observed that a positive E_y is induced in the channel at source/drain sides in both the normal poly-Si TFT and BG poly-Si TFT. Moreover, the value of E_y in the channel of the BG poly-Si TFT is larger than that of the normal poly-Si TFT at the same position. The E_y value at 10 nm below the oxide/channel interface along the drain side to the source side in the normal poly-Si TFT (red line) and BG poly-Si TFT (blue line) is also extracted, as shown in Fig. 8(d). In the normal poly-Si TFT, it can be observed that the E_y value in the channel positively peaks at source/drain sides and decreases toward the center of the channel. In the BG poly-Si TFT, E_y behavior is different. In BG heavily doped regions, the E_y is close to 0 due to the low resistance of BG lines. In the undoped regions, E_y peaks and the maximum

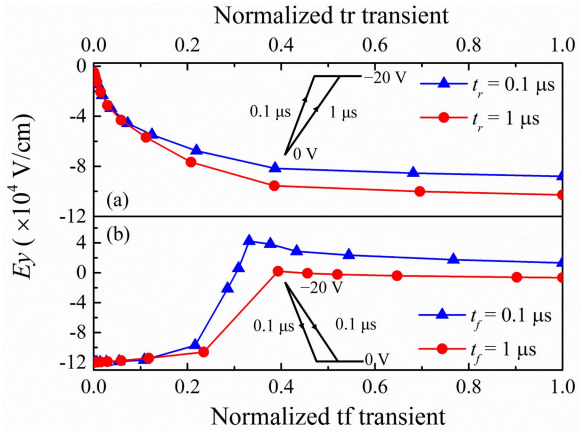

Fig. 9. Dependence of E_y on (a) normalized t_r transient and (b) normalized t_f transient at the channel/drain edge near the gate oxide in a BG poly-Si TFT.

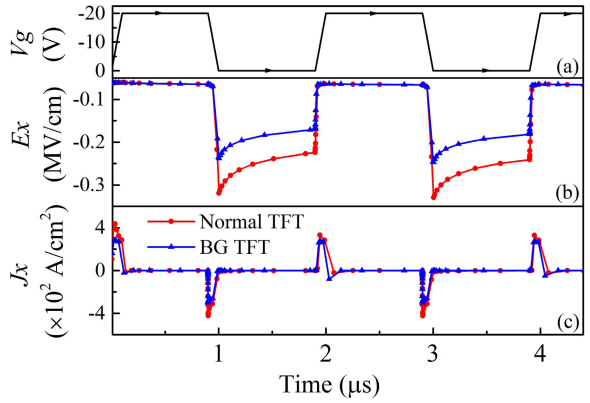

Fig. 10. (a) Dynamic gate pulse applied to the gate electrode. The $t_r = t_f = 0.1$ μs The dependence of (b) E_x and (c) J_x on time at the channel/drain edge. The positive direction is defined from the drain electrode to the source electrode.

positive E_y also appears in the channel at source/drain sides. Furthermore, the value of positive E_y in the channel at the same position in the BG poly-Si TFT is larger than that in the normal poly-Si TFT. From the simulation results, it can be inferred that in the normal poly-Si TFT, electron trapping/injection into the gate oxide only prevails close to the source/drain sides, while in the BG poly-Si TFTs, it may occur in the undoped region in the almost whole channel and prevails close to the source/drain sides. This explains why a larger I_{ON} increase in the first stage is observed in the BG poly-Si TFTs.

Shown in Fig. 9 is the dependence of E_y on the normalized t_r transient and normalized t_f transient at the channel/drain edge near the gate oxide in a BG poly-Si TFT. For t_r, as shown in Fig. 9(a), E_y increases toward the negative direction, resulting in no electron trapping/injection into the gate oxide. Therefore, the I_{ON} increase in the first stage is independent of t_r, as shown in Fig. 5(b). For t_f, as shown in Fig. 9(b), it can be observed that a shorter t_f brings a higher positive E_y, resulting in a larger I_{ON} increase in the first stage, as shown in Fig. 5(b).

When applying a dynamic voltage to the gate electrode, a transient voltage difference in the channel, channel/source edge, and channel/drain edge can be induced [4], [19]. When the dynamic gate stress swings from 0 to −20 V during t_r, the transient voltage difference is negative [Fig. 9(a)], and no electron trapping/injection into gate oxide will occur. Therefore, the I_{ON} increase in the first stage is independent of t_r [Fig. 5(b)]. When the dynamic gate pulse swings from −20 to 0 V during t_f, the transient voltage difference changes toward positive direction. With the assistance of the positive E_y in the later part of t_f, electrons will be trapped/injected into gate oxide, increasing I_{ON}. A faster t_f means a steeper slope of the voltage, resulting a higher E_y [Fig. 9(b)] and thus leading to a larger I_{ON} increase in the first stage [Fig. 5(b)]. For normal poly-Si TFTs, due to the heavily doped source/drain, the electric filed prefers to be shunted to the source/drain, resulting in the occurrence of a peak E_y in the channel/source edge and channel/drain edge, as shown in Fig. 8(d) (red line). For BG poly-Si TFTs, there are a series of heavily doped BG lines inside the active channel. E_y can be shunted to both source/drain regions and the series of heavily doped BG lines, resulting in enhanced E_y in the whole channel, as shown in Fig. 8(d) (blue line). Therefore, the I_{ON} increase in the first stage in BG poly-Si TFTs is larger than that in normal poly-Si TFTs.

In other words, when L decreases, the gate control to the channel becomes weaker. The source/drain is close enough to control the channel. In this paper, the source/drain is grounded during the dynamic gate stress. The potential difference in the y-direction near the source/drain sides becomes larger with shorter L. Therefore, E_y in the channel becomes larger with decreasing L. The BG poly-Si TFT can be treated as several short channel TFTs in series due to the selectively heavily doped BG lines inside the channel. A larger E_y would be induced in the undoped region between the two doped BG regions. Therefore, a larger I_{ON} increase in the first stage in BG poly-Si TFTs is observed.

For the I_{ON} decrease in the second stage, dynamic HC effect is inferred to be responsible. The E_x and carrier are the two essential factors for HC generation [4]–[9], [16]. To analyze the second-stage degradation, a transient E_x and lateral current density (J_x) are simulated, as shown in Fig. 10. For t_r transition, it can be observed that $|E_x|$ decreases sharply. Moreover, J_x is in the opposite direction to E_x. No HCs are generated during t_r [9]. Therefore, the dynamic HC degradation in the second stage is independent of t_r, as shown in Fig. 5(a). For t_f transition, it can be observed that a high E_x is induced and J_x is in the same direction to E_x. Carriers exposed in such high E_x gain enough energy and become HCs. A shorter t_f brings a larger $|E_x|$ [20], resulting in a larger dynamic HC degradation in the second stage. It is also noted that $|E_x|$ in the BG poly-Si TFTs is much smaller than that in the normal poly-Si TFTs, which explains why the second-stage degradation of BG poly-Si TFTs is much smaller than that of normal poly-Si TFTs.

The E_x distributions at the end of t_f in a normal poly-Si TFT and a BG poly-Si TFT are also simulated, as shown in Fig. 11 (inset), and it can be clearly observed that

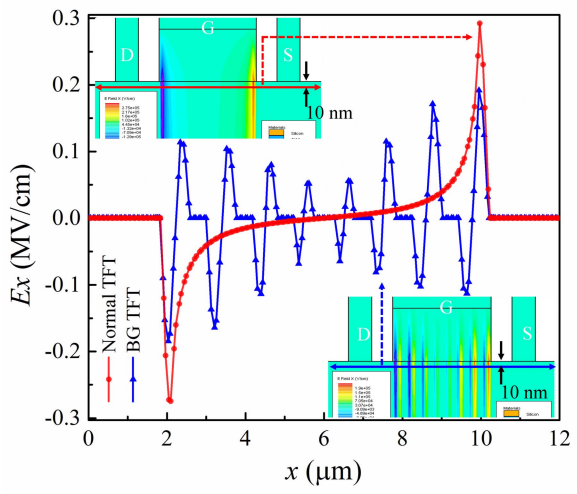

Fig. 11. Extracted E_x at 10 nm below the oxide/channel interface along the source side to the drain side at the end of t_f in a normal poly-Si TFT and a BG poly-Si TFT. Insets: E_x distribution in a normal poly-Si TFT (top) and a BG poly-Si TFT (bottom).

E_x intensity is weakened by BG structure at the source/drain side. To be clearer, E_x is extracted at 10 nm below the oxide/channel interface along the drain side to the source side for both the normal poly-Si TFT (red line) and the BG poly-Si TFT (blue line). The peak value of E_x in BG poly-Si TFTs is significantly reduced, resulting in a better dynamic HC reliability in the second stage in BG poly-Si TFTs.

To clarify the dynamic HC degradation mechanism in the second stage, the nonequilibrium drain junction degradation model [9] is employed and developed. The dynamic stress applied to the gate electrode can induce transient voltage difference between the channel and p^+ source/drain [4], [19]. One may consider that there are two nonequilibrium junctions located at the both channel edges. When the dynamic gate stress swings from 0 to -20 V during t_r, the source/drain junctions become forward biased, and the depletion region of the junctions in the channel will shrink by carrier recombination process from the outer edge of the depletion region [9]. The electric field therein is low, and no HCs are generated. Therefore, the dynamic-gate-stress-induced degradation in the second stage is independent of t_r in poly-Si TFTs. When the dynamic gate stress swings from -20 to 0 V during t_f, the source/drain junctions become reversely biased, and the depletion region of junctions in the channel needs to extend by emitting trap-related carriers. Later emitted carriers from the deep-trap state are exposed to the high E_x across the depletion region and gain enough energy to become HCs. A shorter t_f brings a higher $|E_x|$ in the channel near source/drain side. Meanwhile, only those traps with even shallower energy levels can be emitted within a shorter t_f [9], and a larger part of deep-trap emission will occur after the higher $|E_x|$ is established, resulting in more severe degradation for the shorter t_f. The normal poly-Si TFTs only have two reversed junctions (channel/source junction and channel/drain junction) to share the voltage drop, while the BG poly-Si TFTs have a series of reversed junctions to share the voltage drop, as shown in Fig. 11. Therefore, the dynamic HC degradation in the second stage can be significantly reduced in BG poly-Si TFTs due to the E_x reduction at channel/source edge and channel/drain edge.

Now, the degradation mechanism for both stages is clear in normal poly-Si TFTs and BG poly-Si TFTs. However, one may still wonder how the first-stage degradation transits to the second-stage degradation. In the first stage, electron trapping/injection dominates the device degradation. Such electron trapping/injection at the source/drain sides will reduce the local E_x by dispersion of the electric field lines [9]. Therefore, the dynamic HC degradation is suppressed in the beginning, attributed to the reduced local E_x. As stress time goes on, more and more traps are created in the interface and/or grain boundaries in the channel near the source/drain sides, due to the electron trapping/injection and HCs. With these additional traps located in the depletion region, the source/drain junctions become narrower, and the E_x herein increases. Furthermore, more and more carriers can be emitted from those generated deep traps during t_f. Thus, dynamic HC effect becomes more and more enhanced. A turnaround point will finally appear, and the dynamic HCs begin to dominate the device degradation after the turnaround point. For BG poly-Si TFTs, the larger E_y and the smaller E_x, which are resulted from the heavily doped BG lines inside the active channel, jointly postpone the appearance of the turnaround point.

IV. Conclusion

The degradation behavior and mechanism of BG poly-Si TFTs under dynamic gate stress are systematically characterized and analyzed. A two-stage degradation behavior, related to t_f, is found. The I_{ON} increase in the first stage is dominated by electron trapping/injection into the gate oxide, while the I_{ON} decrease in the second stage is dominated dynamic HC effect. Compared with normal poly-Si TFTs, BG poly-Si TFTs exhibit much more reliable characteristic in terms of larger I_{ON} increase in the first stage and much smaller I_{ON} decrease in the second stage. The larger I_{ON} increase in the first stage and the smaller I_{ON} decrease in the second stage in BG poly-Si TFTs are, respectively, attributed to enhanced E_y along the channel near the gate oxide and reduced E_x caused by the sharing of the field across multiple reversely biased junctions. The degradation mechanism in both first stage and second stage is clarified. Besides this, the impact of the first-stage degradation on the second-stage degradation is also explained. All test results indicate that these high-performance BG poly-Si TFTs with good static/dynamic reliability have great potential for SoP application in the future.

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