Characterization of DC-Stress-Induced Degradation in Bridged-Grain Polycrystalline Silicon Thin-Film Transistors

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***Abstract*— In this paper, dc-stress-induced degradation in bridged-grain (BG) polycrystalline silicon (poly-Si) thin-film transistors (TFTs) is systemically characterized and investigated. Compared with normal poly-Si TFTs, BG poly-Si TFTs exhibit better hot-carrier (HC) reliability, better self-heating (SH) reliability, and better negative bias temperature (NBT) instability. Resulting from the heavily doped BG lines inside the active channel, lateral electric field reduction at the drain side, Joule heat diffusion enhancement at the channel length direction, and boron–hydrogen bond formation at interface/grain boundaries are, respectively, responsible for the improved HC reliability, SH reliability, and NBT reliability in BG poly-Si TFTs. In addition, stress V_g-dependent HC degradation with fixed stress V_d, stress power density-dependent SH degradation, and vertical electrical field-dependent NBT degradation are also examined in both normal poly-Si TFTs and BG poly-Si TFTs. All test results indicate that such high-performance and highly reliable BG poly-Si TFT has a great potential for system-on-panel application.**

***Index Terms*— Bridged grain (BG), hot carrier (HC), negative bias temperature instability (NBTI), polycrystalline silicon (poly-Si), self-heating (SH), thin-film transistors (TFTs).**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have received considerable attention in active-matrix liquid crystal displays and organic light emitting diode displays due to their ability to integrate pixel elements with driving circuits to achieve the system-on-panel (SOP) application [1]. High-performance poly-Si TFTs with good reliability are thus required to accomplish the above purpose. In the past few decades, different kinds of treatments on active channel [2]–[5] have been proposed and applied to fabricate high-performance poly-Si TFTs, such as plasma passivation [2], high-temperature annealing [3], and nanostructure/microstructure configurations [4], [5]. However, these methods either bring process variation/reliability issues [2] or are incompatible with the low-temperature process/standard process in the industry [3]–[5]. Recently, bridged-grain (BG) technology [6]–[9] has been proposed and introduced to generate high-performance poly-Si TFTs. By selectively doping BG lines inside the active channel [6]–[9], grain size effect, short-channel effect (SCE), and multijunction effect are beneficially exploited, resulting in excellent device electrical characteristics in terms of field-effect carrier mobility (μ_{FE}), threshold voltage (V_{th}), subthreshold swing (SS), and ON-current/OFF-current ratio ($I_{\mathrm{ON}}/I_{\mathrm{OFF}}$). For these high-performance BG poly-Si TFTs, hitherto no systematical reliability studies have been performed and reported.

It has been identified for poly-Si TFTs that hot-carrier (HC) effect [10]–[14], self-heating (SH) effect [15]–[22], and negative bias temperature instability (NBTI) effect [23]–[27] are three key mechanisms inducing device degradation. In this paper, degradation of BG poly-Si TFTs under different kinds of dc stresses [HC stress, SH stress, and negative bias temperature (NBT) stress], is symmetrically investigated. Compared with the normal poly-Si TFTs, BG poly-Si TFTs exhibit better HC reliability, better SH reliability, and better NBT reliability, which are mainly attributed to the lateral electric field (E_x) reduction at drain side, improved Joule heat diffusion at channel length (L) direction, and boron–hydrogen (B–H) bond formation in the channel, respectively. In addition, for HC degradation, it is found that stress V_g-dependent device degradation in p-type poly-Si TFTs is different from that in n-type poly-Si TFTs. With fixed stress V_d, larger stress $|V_g|$ brings more device degradation in p-type poly-Si TFTs. For SH degradation, longer L brings more severe degradation at the same stress power density (p) and electric field in gate oxide (E_{ox}). For NBT degradation, it is independent of L when $L > \sim 5$ μm and decreases with decreasing L when $L < \sim 5$ μm.

II. Experiment

Four-inch sized silicon wafers covered with 500-nm-thick thermal oxide were applied as the starting substrates and 50-nm-thick amorphous silicon (a-Si) was deposited onto the substrate through low-pressure chemical vapor deposition (LPCVD) at 550 °C as the active layer. Then, 5-nm-thick nickel (Ni) was evaporated onto the surface of a-Si layer, followed by nitrogen annealing at 600 °C for 6 h to convert the a-Si film into a poly-Si film. After annealing, the wafer was treated by sulfuric acid cleaning to remove Ni. Then, 50-nm-thick low-temperature oxide (LTO) was

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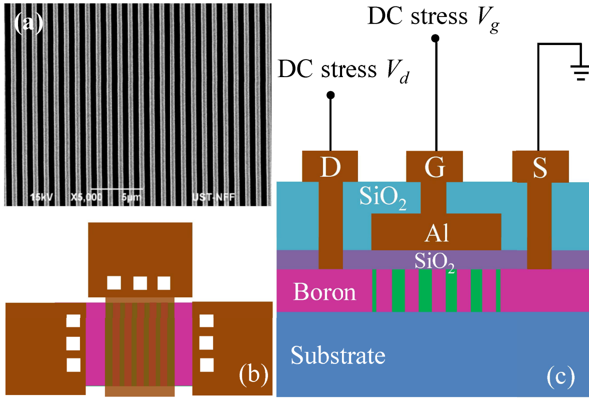

Fig. 1. (a) SEM image of PR pattern of BG lines. (b) Top-down view of a BG poly-Si TFT. (c) Cross-sectional schematic of a BG poly-Si TFT and stress conditions.

deposited by LPCVD at 425 °C, which would serve as the sacrificial layer for BG ion implantation. Next, a layer of photoresist (PR) was spin coated and patterned into gratings with a period of 1 μm and an aspect ratio of 50%. Structures of the patterned PR captured by the scanning electron microscope (SEM) are shown in Fig. 1(a). Boron (B) implantation with a dose of $2 \times 10^{15}/\text{cm}^2$ was performed to the exposed areas through the gratings. After implantation, the PR and LTO sacrificial layer were removed, followed by active island patterning. Then, 70-nm-thick SiO_2 deposited by LPCVD at 425 °C is employed as gate dielectric. After gate dielectric deposition, 300-nm-thick aluminum (Al) was subsequently sputtered and patterned as gate electrodes. The source and drain were formed by a self-aligned B implantation at a dosage of $5 \times 10^{15}/\text{cm}^2$. After formation of the source/drain, a 500-nm-thick LTO layer was deposited as an isolation layer. The contact holes were defined and 700-nm-thick Al–1%Si was subsequently sputtered and patterned as testing pads. The devices were then sintered in forming gas for 30 min at 420 °C. No further passivation was applied to these devices. The top-down view and cross-sectional schematic of a BG TFT is shown in Fig. 1(b) and (c), respectively. For comparison, normal poly-Si TFTs were also fabricated at the same time by going through the same processes only without the BG treatment.

For poly-Si TFTs under test, the channel width (W) is fixed at 10 μm. The L of normal poly-Si TFTs is varied from 0.5 to 20 μm while for BG poly-Si TFTs, the L is fixed at 12 μm. Due to dopant lateral penetration [9] when performing ion implantation to form BG lines, the effective L (L_{eff}) of BG poly-Si TFTs with $L = 12$ μm would be smaller than $L/2 = 6$ μm. By utilizing TSUPREM-4 simulation, the L_{eff} of BG poly-Si TFTs with $L = 12$ μm is estimated as ~5.5 μm, a little bit smaller than 6 μm. The L_{eff} of normal poly-Si TFTs approximately equals to L. For comparison between normal poly-Si TFTs and BG poly-Si TFTs with the same L_{eff}, the L_{eff} of BG poly-Si TFTs with $L = 12$ μm is approximately treated as 6 μm. Device is stressed and characterized before and after stress using HP 4156A semiconductor parameter analyzer. The μ_{FE} is extracted from the following expressions [1]:

$$\mu_{\text{FE}} = \frac{LdG_m}{W\varepsilon_{\text{ox}}V_{\text{ds}}}$$

where d, ε_{ox}, and G_m are physical gate dielectric thickness, gate dielectric permittivity, and maximum of transconductance at $V_{\text{ds}} = -0.1$ V. I_{ON} is defined at $V_g = -22$ V and V_{th} is determined by the interception of linear extrapolation of a transfer curve at $V_{\text{ds}} = -0.1$ V. The subthreshold slope (SS) is also extracted at $V_{\text{ds}} = -0.1$ V from the slope of log $|I_{\text{ON}}|$ in the subthreshold region. The $I_{\text{ON}}/I_{\text{OFF}}$ ratio equals to maximum current over minimum current within the measured range. The E_{ox} is approximated as $(V_g - V_{\text{mg}})/d$ [22], [28], where V_{mg} stands for midgap voltage, evaluated as the gate voltage giving a drain current around 1 pA [22]. Three groups of stresses, namely dc HC stress, dc SH stress, and dc NBTI stress, are applied to evaluate the reliability of normal poly-Si TFTs and BG poly-Si TFTs. For the dc HC stress, the stress conditions are set with fixed stress V_d of −40 V, varied stress V_g from −5 to −25 V, and grounded source electrode. For the dc SH stress, the stresses V_d and V_g are conditionally varied at the same time ($|V_g - V_{\text{th}}| > |V_d|$) to keep both normal poly-Si TFTs and BG poly-Si TFTs in the linear region to avoid HC generation near the drain side. The stress conditions are set with varied stress V_d from −6.8 to −26 V, correspondingly varied stress V_g from −27 to −40 V and grounded source electrode, which leads to a varied p from 18.9 to 113.8 $\mu\text{W}/\mu\text{m}^2$ and a varied E_{ox} from −3.5 to −4.6 MV/cm. For the dc NBTI stress, the stress conditions are set with varied V_g from −25 to −45 V and grounded source/drain electrodes, which leads to a varied E_{ox} from −3.2 to −5.3 MV/ cm. All device reliability tests are performed at room temperature (23 °C) without light illumination. Device degradation is characterized by a percentile change in I_{ON} with respect to its initial value (ΔI_{ON}) and V_{th} shift.

III. Results and Discussion

Fig. 2 shows the transfer curve comparison between normal poly-Si TFTs and BG poly-Si TFT. For the same $L = 12$ μm, compared with the normal poly-Si TFT, apparently the BG poly-Si TFT exhibits much better electrical characteristics in terms of I_{ON}, SS, I_{OFF}, and V_{th}. For the same $L_{\text{eff}} = 6$ μm, again all device parameters of the BG poly-Si TFT are better than the normal poly-Si TFT. The key device parameters of normal poly-Si TFTs and BG poly-Si TFTs are summarized in Table I. These great improvements achieved by utilizing the BG structure are mainly attributed to grain size effect, SCE and multijunction effect [6]–[9]. For grain size effect, the doped BG region inside the channel could reduce grain boundary (GB) traps [7], [29] and lower the GB barrier along the current path. Extracted from the inset of Fig. 2 using the Proano and Levinson method [30], [31], the GB trap state density (N_t) for normal poly-Si TFT and BG poly-Si TFT are 3.48×10^{12} and 2.98×10^{12} cm^{-2}, respectively. Consistent to the above point, the GB N_t dose can be reduced by BG lines. In other words, the BG regions could provide shortcuts to the carriers and help these carriers find the more conductive path,

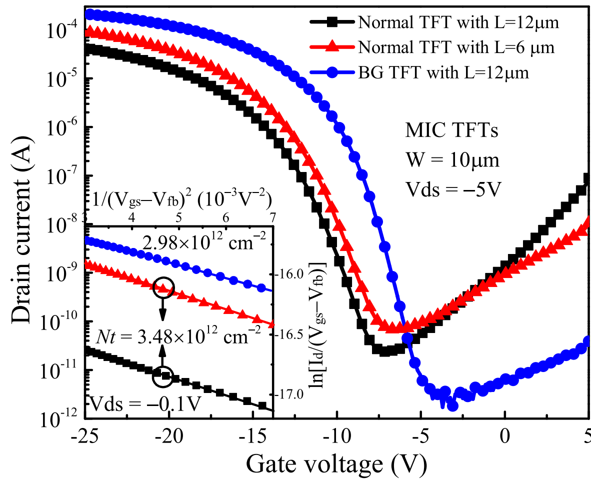

Fig. 2. Transfer curve comparison among the normal poly-Si TFT with $L = 12\ \mu$m, the normal poly-Si TFT with $L = 6\ \mu$m, and the BG poly-Si TFT with $L = 12\ \mu$m. The inset is $\ln[I_d/(V_{gs} - V_{fb})]$ versus $1/(V_{gs} - V_{fb})^2$ curves at $V_{ds} = -0.1$ V and high V_{gs} for normal poly-Si TFTs and the BG poly-Si TFT.

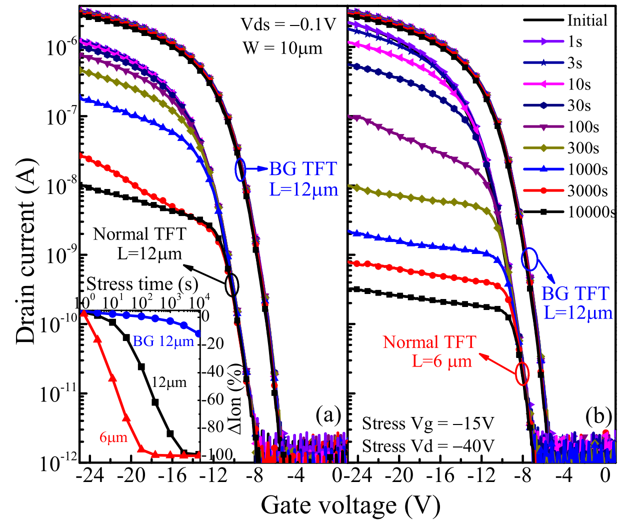

Fig. 3. Transfer curve degradation comparison between the normal poly-Si TFT and the BG poly-Si TFT for (a) $L = 12\ \mu$m and (b) $L_{\text{eff}} = 6\ \mu$m under the same HC stress. The inset is I_{ON} degradation dependent on stress time for normal poly-Si TFTs and the BG poly-Si TFT.

TABLE I

EXTRACTED DEVICE PARAMETERS FROM NORMAL POLY-SI TFTS AND BG POLY-SI TFTS AT $V_{ds} = -0.1$ V

Parameters	Normal TFT with *L*=6μm	Normal TFT with *L*=12μm	BG TFT with *L*=12μm
μ_{FE} (cm²/Vs)	26.9	26.8	64.6
V_{th} (V)	−13.4	−13.4	−8.4
SS (V/dec)	1.1	1.1	1.0
I_{on}/I_{off} (at V_{ds}=−5V)	1.5×10⁶	1.6×10⁶	1.2×10⁸
GB N_t (cm⁻²)	3.5×10¹²	3.5×10¹²	3.0×10¹²

resulting in improved I_{ON}, SS, I_{OFF}, and V_{th} [6], [8]. For SCE, it is beneficially employed for I_{ON} improvements, resulting in higher I_{ON} and smaller V_{th} [9]. For multijunction effect, it is inherent in the BG structure and it can efficiently suppress the I_{OFF} [8], [9].

A. Hot Carrier

Fig. 3(a) shows the transfer curve degradation of normal poly-Si TFTs and the BG poly-Si TFT under the same HC stress. For normal poly-Si TFTs, typical HC degradation behaviors [12]–[14], decreased I_{ON} and unchanged SS, are observed. Carriers are exposed to high E_x generated by applied stresses and therefore gain enough energy to become HCs, creating defects at the GBs/interface at the drain side and thus increasing trap potential [14]. For the same $L = 12\ \mu$m, as shown in Fig. 3(a), the BG poly-Si TFT shows much better HC reliability compared with the normal poly-Si TFT under the same HC stress. The extracted ΔI_{ON} is shown in the inset. After 10^4 s stress, the ΔI_{ON} of the normal poly-Si TFT is almost 100% while for the BG poly-Si TFT ΔI_{ON} is only less than 12%. To make the comparison more reasonable, HC degradation of the normal poly-Si TFT and the BG poly-Si TFT for the same $L_{\text{eff}} = 6\ \mu$m is also examined, as shown in Fig. 3(b). Similar to the same $L = 12\ \mu$m, the BG poly-Si TFT is much more stable under the same HC stress compared with the normal poly-Si TFT. In addition, for normal poly-Si TFTs,

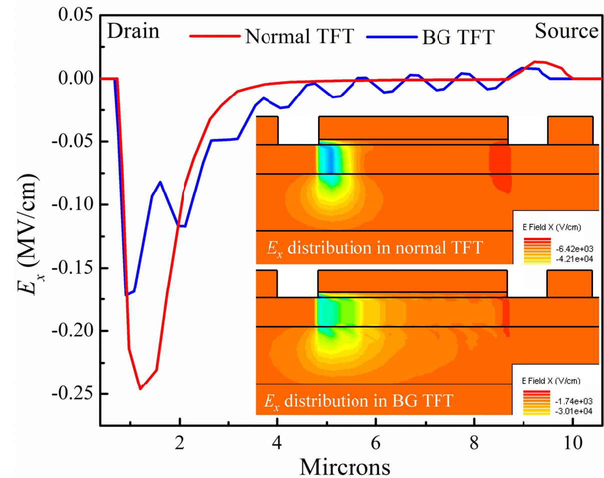

Fig. 4. Extracted E_x at 5 nm below oxide/channel interface along the drain side to the source side under the HC stress in a normal poly-Si TFT and a BG poly-Si TFT. The inset is E_x distribution in a normal poly-Si TFT and a BG poly-Si TFT.

shorter L brings larger HC degradation, which is attributed to higher E_x for shorter L under the same HC stress [14]. For the improved HC reliability in BG poly-Si TFTs, E_x reduction by BG lines at the drain side may be responsible.

To verify the above point, E_x simulation under HC stress in a normal poly-Si TFT and a BG poly-Si TFT was performed using Silvaco Atlas based on a continuous defect poly-Si model, as shown in Fig. 4. Shown in the inset are E_x distributions in a normal poly-Si TFT and a BG poly-Si TFT. It can be observed that E_x intensity is weakened by BG structure at the drain side. To be clearer, E_x is extracted at 5 nm below the oxide/channel interface along the drain side to the source side for both the normal poly-Si TFT (red line) and the BG poly-Si TFT (blue line). Apparently, the peak of E_x, which is the essential factor for HC generation [10]–[14] is reduced by BG structure, resulting in better HC reliability in BG poly-Si TFTs.

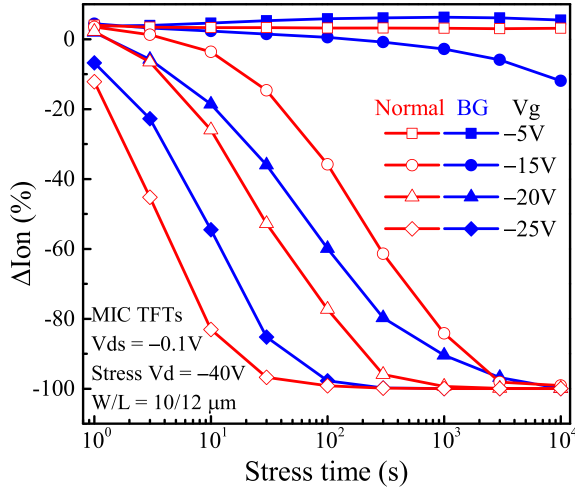

Fig. 5. I_{ON} degradation dependent on stress time at various V_g bias with fixed stress $V_d = -40$ V in normal poly-Si TFTs and BG poly-Si TFTs.

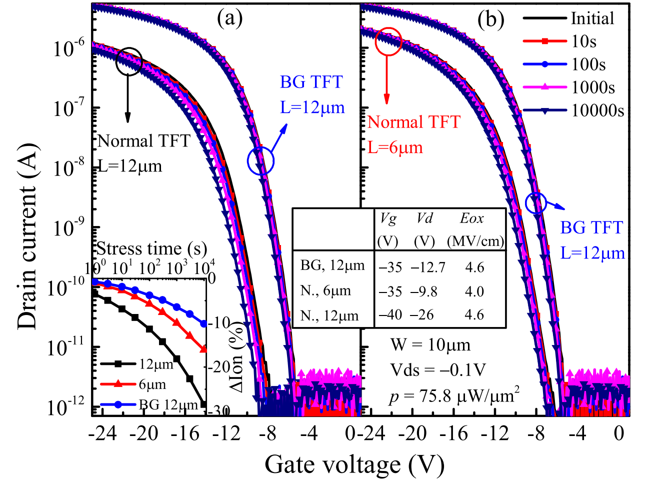

Fig. 6. Transfer curve degradation comparison between the normal poly-Si TFT and the BG poly-Si TFT for (a) $L = 12$ μm and (b) $L_{\text{eff}} = 6$ μm under the same p. The inset is I_{ON} degradation dependent on stress time for normal poly-Si TFTs and the BG poly-Si TFT.

The I_{ON} degradation dependent on stress time at various stress V_g with fixed stress $V_d = -40$ V is also examined in normal poly-Si TFTs (red lines) and BG poly-Si TFTs (blue lines), as shown in Fig. 5. For the ON-state stress (stress $|V_g| >$ stress $|V_{\text{th}}|$), apparently the degradation of BG poly-Si TFTs is smaller than that of normal poly-Si TFTs for each fixed V_g stress, indicating better reliability of BG poly-Si TFTs. It is also noted that for both normal poly-Si TFTs and BG poly-Si TFTs, larger stress $|V_g|$ brings more severe I_{ON} degradation, which is different from that in n-type poly-Si TFTs [10], [12]. In n-type poly-Si TFTs under the fixed stress V_d, the V_g dependent of HC degradation is a bell-shaped dependence [12] and the largest HC degradation occurs when stress V_g is around V_{th}, which is due to the reduction of E_x by increasing stress V_g if $V_g > V_{\text{th}}$ [10]. However, for p-type poly-Si TFTs, when increasing stress $|V_g|$ in a negative direction, NBTI would be involved in the source side [26] and thus enhance the total degradation [25], [26]. For the OFF-state stress (stress $|V_g| <$ stress $|V_{\text{th}}|$), it is observed that no HC degradation occurs and I_{ON} is slightly increased instead of decreased. Since stress $|V_g| <$ stress $|V_{\text{th}}|$, no holes will be induced in the channel and therefore no HCs are generated. Such a slight increase in I_{ON} is mainly attributed to negative charges trapped in the gate oxide near the drain side [14], [32].

B. Self-Heating

The SH degradation depends upon Joule heating generated by high-stress power [15]–[20] and upon E_{ox} generated by stress V_g [22]. Therefore, to make the SH degradation comparison between normal poly-Si TFTs and BG poly-Si TFTs more fair, the stress power density p, which equals to stress power divided by the area of the channel, and E_{ox} are employed for the SH discussion.

Fig. 6 shows comparison of transfer curve degradation among normal poly-Si TFTs and the BG poly-Si TFT at the same $p = 75.8$ $\mu W/\mu \text{m}^2$. It can be observed that SH stress, unlike HC stress, brings degradation in both ON-state region and subthreshold region. High power combined with high $|E_{\text{ox}}|$ could distort/break some of strong Si–Si bonds located at GBs in the whole channel [16], [22] and break Si–H bonds at interface/GBs [19], [22], resulting in the regeneration of dangling bonds in the channel layer and positive oxide charge generation, and thus decreasing I_{ON} and shifting V_{th}. For the same $L = 12$ μm, as shown in Fig. 6(a), at the same p and E_{ox}, the BG poly-Si TFT exhibits better SH reliability than the normal poly-Si TFT. For the same $L_{\text{eff}} = 6$ μm, as shown in Fig. 6(b), at the same p, the BG poly-Si TFT again exhibits better SH reliability although the BG poly-Si TFT suffers from higher $|E_{\text{ox}}|$. To alleviate the SH effect, one of effective methods is to dissipate the heat quickly [15], [17], [19]. For the BG poly-Si TFT, the BG lines inside the channel are heavily doped and have low resistance, where almost no Joule heat could be generated. Therefore, the heat diffusion at L direction could be greatly promoted [17], resulting in alleviated SH degradation in BG poly-Si TFTs. On the other hand, since a part of SH degradation occurs at GBs, the less GB N_t of unstressed BG ploy-Si TFTs may also contribute to the alleviation of SH degradation. In addition, it is also observed that for normal poly-Si TFTs, as clearly shown in the inset, longer L brings more severe SH degradation at the same p. This is partly attributed to the geometric effect [19], [20], [22] and partly attributed to the higher $|E_{\text{ox}}|$ that normal poly-Si TFT with $L = 12$ μm suffers from.

I_{ON} degradation dependent on p at various E_{ox} for normal and BG poly-Si TFTs is also examined, as shown in Fig. 7. Unsurprisingly, a larger p combined with higher $|E_{\text{ox}}|$ brings more severe SH degradation for both normal poly-Si TFTs and BG poly-Si TFTs. For varied p with the same $|E_{\text{ox}}| = 4.6$ MV/cm, larger SH degradation for lager p is also observed for both normal and BG poly-Si TFTs. However, compared with the degradation slope for a large p combined with high $|E_{\text{ox}}|$, the SH degradation slope for varied p and the fixed E_{ox} in both normal poly-Si TFTs and BG poly-Si TFTs become slow, which is due to both p and E_{ox} jointly enhance the SH degradation [22]. At the same p and E_{ox}, consistent to the data shown in Fig. 6, BG poly-Si TFT

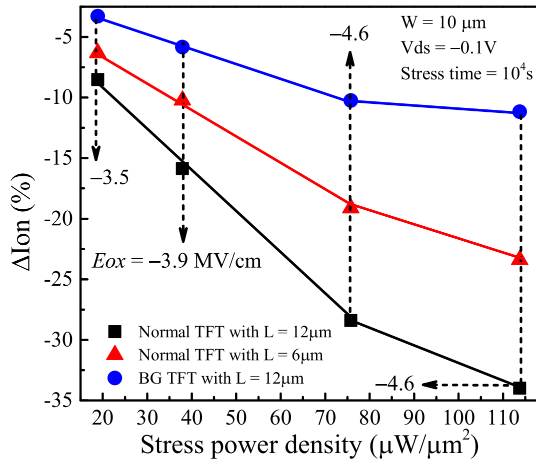

Fig. 7. I_{ON} degradation dependent on p at various E_{ox} for normal poly-Si TFTs and BG poly-Si TFTs.

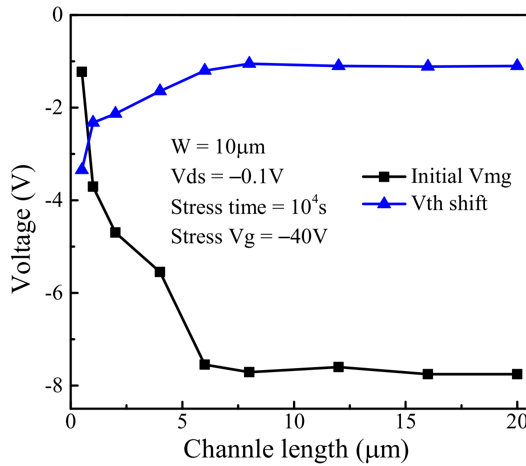

Fig. 8. V_{mg} dependent on L before NBT stress and V_{th} shift dependent on L after NBT stress in normal poly-Si TFTs.

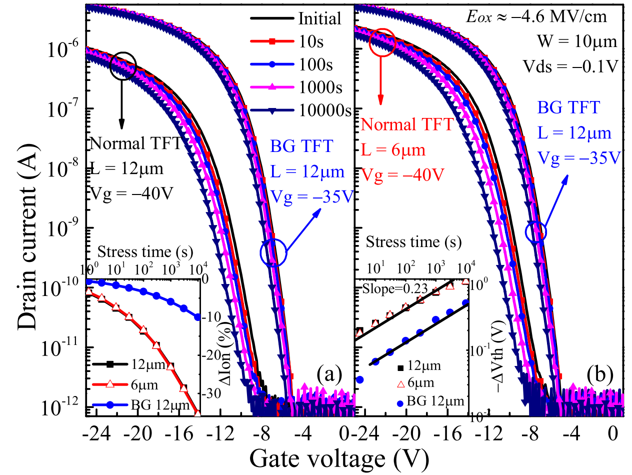

Fig. 9. Transfer curve degradation comparison between the normal poly-Si TFT and the BG poly-Si TFT for (a) $L = 12\ \mu$m and (b) $L_{\mathrm{eff}} = 6\ \mu$m under NBT stress. The left and right insets are I_{ON} degradation and V_{th} shift dependent on stress time for normal\BG poly-Si TFTs, respectively.

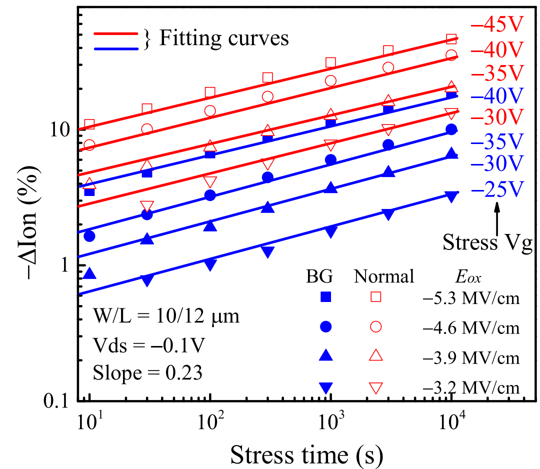

Fig. 10. I_{ON} degradation dependent on stress time at various E_{ox} for normal poly-Si TFTs and BG poly-Si TFTs.

does exhibit better SH reliability and larger L brings more SH degradation.

C. Negative Bias Temperature Instability

Fig. 8 shows V_{mg} dependent on L before NBT stress and V_{th} shift dependent on L after NBT stress in normal poly-Si TFTs. For V_{mg} (black line), it can be observed that $|V_{mg}|$ keeps a constant when $L > \sim 5\ \mu$m and then decreases with decreasing L when $L < \sim 5\ \mu$m. After 10^4 s stress $V_g = -40$ V, the V_{th} shift (blue line) is kept the same for $L > \sim 5\ \mu$m but is enhanced by shorter L for $L < \sim 5\ \mu$m, which holds similar trend as L-dependent V_{mg}. For the enhanced NBTI for $L < \sim 5\ \mu$m, it may be due to the $|E_{ox}|$ increase by $|V_{mg}|$ reduction. On the other hand, the NBT degradation is more severe at channel edge [23]. Therefore, shorter L device should be more sensitive to the damage near the source/drain region [23], partly resulting in L-dependent NBT degradation in short L TFTs. To eliminate the V_{mg} variation induced degradation and channel edge related degradation in normal poly-Si TFTs and BG poly-Si TFTs, for both normal poly-Si TFTs and BG poly-Si TFTs, E_{ox} generated by stress V_g is kept the same and TFTs with large L ($> \sim 5\ \mu$m) are chosen.

Fig. 9 shows comparisons of transfer curve degradation in normal poly-Si TFTs and BG poly-Si TFTs under NBT stress. Typical NBT degradation behaviors, negative V_{th} shift and the degradation slope of 0.23 [1], [24], [26], [27], are observed, as shown in Fig. 9 and its right inset. Trap state generation at interface/GBs and fixed oxide charge generation [24]–[27] are responsible for NBT degradation. Fig. 9(a) shows the transfer curve degradation of normal and BG poly-Si TFTs for the same $L = 12\ \mu$m. It can be observed that V_{th} shift of the BG poly-Si TFT is smaller than that of normal TFT, indicating better NBT reliability. For the same $L_{\mathrm{eff}} = 6\ \mu$m, as shown in Fig. 9(b), the BG poly-Si TFT again shows better NBT reliability. For NBT degradation, both trap state generation and fixed charge formation originate from the depassivation of weak Si–H bonds located at interface/GBs [24]–[27]. By selectively doping the active channel with boron, hydrogen localization near boron in

poly-Si may happen by formation of B–H [33], [34], and the B–H bond dissociation energy is larger than Si–H [35]. Therefore, under the same E_{ox}, a smaller part of hydrogen is dissociated, resulting in better NBT reliability. Furthermore, the lower GB N_t of unstressed BG poly-Si TFTs may also contribute to the better NBTI. In addition, for normal poly-Si TFTs, NBT degradation is independent of $L(L > 5\ \mu\mathrm{m})$, as shown in insets in Fig. 9, consistent to the previous data shown in Fig. 8.

NBT degradation under different E_{ox} for normal poly-Si TFTs and BG poly-Si TFTs is also examined, as shown in Fig. 10. The degradation slope equals to ∼0.23 and larger $|E_{\mathrm{ox}}|$ brings larger NBT degradation. Clearly, at the same $|E_{\mathrm{ox}}|$, BG TFTs exhibit better NBT reliability compared with the normal TFTs. It is noteworthy that BG poly-Si TFTs also exhibit better NBT reliability even at the same stress V_g.

IV. Conclusion

Degradation behaviors and mechanisms of BG poly-Si TFTs under different kinds of dc stresses are characterized and discussed. Compared with the normal poly-Si TFTs, BG poly-Si TFTs exhibit better HC reliability, better SH reliability, and better NBT reliability. All reliability improvements in BG poly-Si TFTs derive from the heavily doped BG lines inside the active channel. The E_x reduction at the drain side, faster Joule heat diffusion at L direction, and the B–H formation at interface/GBs account for the better HC reliability, SH reliability, and better NBTI, respectively. All the test results suggest that such high-performance BG poly-Si TFTs with excellent reliability have great potential in SOP applications in the future.

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