A Simple Method to Grow Thermal SiO_2 Interlayer for High-Performance SPC Poly-Si TFTs Using Al_2O_3 Gate Dielectric

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***Abstract*— A simple method is proposed to grow thermal SiO_2 interlayer when performing solid-phase-crystallized (SPC) process. By employing such interlayer between SPC polycrystalline silicon channel and Al_2O_3 gate dielectric, high-performance SPC thin-film transistors (TFTs) with field effect mobility of 67.80 $cm^2V\ s^{-1}$ and ON/OFF ratio of 2.31 × 10^8 at V_{ds} = −0.1 V are achieved due to the superior interface quality and improved grain boundaries by the incorporation of excess Si interstitials. The TFT with interlayer also exhibits good reliability under negative bias temperature stress test.**

***Index Terms*— Solid-phase-crystallized, polycrystalline silicon, thin-film transistor, thermal SiO_2, Al_2O_3, interlayer.**

I. Introduction

LOW temperture polycrystalline silicon (poly-Si) thin film transistors (TFTs) are of significant importance for high-resolution flat-panel displays since they have great potential to realize system-on-panel (SOP) application by integrating pixel switching elements and peripheral circuits on a glass substrate [1]. High-performance poly-Si TFTs fabricated at low temperature with large carrier mobility, small threshold voltage (V_{th}) and high current on-off ratio (I_{on}/I_{off}) are thus required to accomplish the SOP purpose. High quality channel/dielectric interface [2]–[5] and high-*k* dielectrics [6]–[9] are two essential factors for the fabrication of high-performance poly-Si TFTs. For interface quality improvement, several methods [2]–[5], such as employing chemical mechanical polished poly-Si film [2], utilizing selective etching [3], inserting buffer layers [4] between channel/gate dielectric and using temperature annealing [5], have been proposed and implemented in the high-performance TFT fabrication. However, these methods either increase process complexity/manufacture cost [2]–[4] or are incompatible with low temperature process [5]. For high-*k* dielectrics, a number of materials [6]–[9], such as Al_2O_3 [6], $LaAlO_3$ [7], HfO_2 [8] and Pr_2O_3 [9], are applied into poly-Si TFTs to improve

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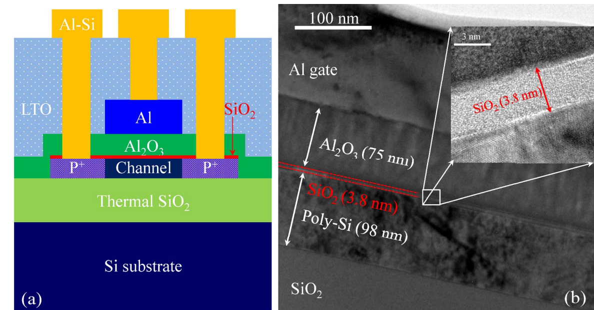

Fig. 1. (a) Schematic cross section of the proposed SPC poly-Si TFT with thermal SiO_2 buffered Al_2O_3 gate dielectric. (b) TEM image of the proposed gate structure.

device characteristic. Among these high-*k* materials, Al_2O_3 thin film deposited by magnetron sputtering technique has great potential [10] for the mass production in industry due to its high deposition rate, large area, good uniformity and low cost.

In this letter, a simple method, which does not increase process complexity at all and is completely compatible with low temperature process, is introduced to grow thermal SiO_2 interlayer between solid-phase-crystallized (SPC) poly-Si channel and the magnetron-sputtered Al_2O_3 gate dielectric for high-performance SPC poly-Si TFT. By employing such thermal SiO_2 interlayer, the proposed TFT shows great improvements in terms of field effect carrier mobility (μ_{FE}), subthreshold slope (*SS*), V_{th}, and I_{on}/I_{off}. Furthermore, negative bias temperature instability (NBTI) degradation of proposed TFT is also greatly alleviated.

II. Experiment

The schematic cross section of the proposed SPC poly-Si TFT with thermal SiO_2 buffered Al_2O_3 gate dielectric is depicted in Fig. 1(a). Fabrication of the TFTs started with the formation of 500nm-thick thermal oxide on 4-inch c-Si wafers. First, a layer of amorphous-Si (a-Si) film was deposited by low-pressure chemical vapor deposition (LPCVD). Active island pattern was subsequently performed, followed by SPC process. Two kinds of SPC process was used to crystallize the a-Si film. One is the standard SPC process [6] carried out at 600 °C for 24h in N ambient on the control wafer for comparison and the other is the proposed SPC process carried

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out at 600 °C for 24h in O_2 ambient. The pressure for both SPC processes was fixed at 760Torr. By replacing N_2 ambient by O_2 ambient during SPC process, 3.8nm-thick thermal SiO_2 was obtained, which would serve interlayer between poly-Si channel and Al_2O_3 dielectric. The next step was the deposition of Al_2O_3 gate dielectric. Before the deposition, 30s HF dip ($HF:H_2O = 100:1$) was performed to the control wafer to remove the native oxide/nitride on the top of poly-Si islands. After the treatment, 75nm-thick Al_2O_3 was deposited using reactive DC magnetron sputtering method in a mixed Ar and O_2 ambient ($Ar/O_2 = 25/3$), with a power density $6W/cm^2$ and a deposition pressure of 3mTorr. Then 300nm-thick aluminum was sputtered and patterned as gate electrode. Next, self-aligned 35keV boron implantation was done at a dosage of $4\times 10^{15}cm^{-2}$. After implantation, 500nm-thick SiO_2 was then deposited by LPCVD as passivation layer, followed by contact hole definition. After the contact hole definition, 700nm-thick Al-1%Si was sputtered and patterned as electrodes. Finally, the wafers were sintered in forming gas for 30min at 420 °C. No further passivation treatments were applied to these wafers.

For characterizations, transmission electron microscopy (TEM) is employed to examine device cross section. Device transfer/output curves and CV curves are characterized by the Agilent 4156B and the Agilent 4284A respectively. The μ_{FE} is extracted from the following expressions [6],

$$\mu_{FE} = \frac{LdG_m}{W\varepsilon_{ox}V_{ds}} \quad (1)$$

where L, W, d, ε_{ox}, and G_m are channel length, channel width, physical gate dielectric thickness, gate dielectric permittivity, drain current and maximum of transconductance at $V_{ds} = -0.1V$. The V_{th} is determined by the interception of linear extrapolation of a transfer curve at $V_{ds} = -0.1V$. The SS is also extracted at $V_{ds} = -0.1V$ from the slope of log $|I_{on}|$ in the subthreshold region. The I_{on}/I_{off} ratio equals to maximum current over minimum current within the measured range. Devices in the test have $24\mu m$ in W and $10\mu m$ in L.

III. Results and Discussion

The relative permittivity of Al_2O_3 is calculated to be 8.14 by measuring the capacitance density of Si/53nm-thick-Al_2O_3/Al capacitor with area of $50\mu m \times 50\mu m$. The equivalent oxide thickness (EOT) of Al_2O_3 gate dielectric with and without interlayer is calculated as 39.73nm and 35.93nm respectively. The cross-sectional TEM image of the proposed SPC poly-Si TFT with thermal SiO_2 buffered Al_2O_3 gate dielectric is shown in Fig. 1(b). The thicknesses of Al_2O_3 and poly-Si are 75nm and 98nm respectively. The interlayer, which is the thermal SiO_2 grown during SPC process, is about 3.8nm.

The transfer characteristics of the proposed SPC TFT using SiO_2/Al_2O_3 gate dielectric and TFT using Al_2O_3 gate dielectric are shown in Fig. 2(a). Compared to SPC TFT with SiO_2 gate dielectric [6], by employing high-k Al_2O_3 (red lines in Fig. 2), all the device parameters of TFT are improved except the gate induced drain leakage (GIDL) current [11], as summarized in Table I. The thinner EOT with the same physical thickness of high-k Al_2O_3 gate dielectric increases gate capacitance and improves the mobile carrier density, resulting in smaller V_{th} and SS [6]–[9]. The GIDL current of TFT with Al_2O_3 gate dielectric is larger than that of TFT with SiO_2 gate dielectric [6], which is caused by the higher electric field at the drain junction owing to the larger gate capacitance density of the high-k Al_2O_3 gate dielectric [6], [9]. For the proposed SPC poly-Si TFT with thermal SiO_2 buffered Al_2O_3 gate dielectric (blue lines in Fig. 2), all electrical parameters are improved, compared to TFT only with Al_2O_3 gate dielectric and TFT with SiO_2 dielectric [6], especially for I_{on} and I_{off}. As summarized in Table I, the μ_{FE} of TFT with interlayer is 67.80 cm^2 Vs^{-1}, 2.76 times larger than that of TFT without interlayer. The V_{th} and SS of TFT with interlayer are improved from -5.18 to $-3.78V$ and from 0.76 to 0.62 V dec^{-1}, respectively. The I_{on}/I_{off} at $V_{ds} = -5V$ is enlarged from 2.74×10^4 to 1.87×10^6, almost 68 times larger than that of TFT without interlayer. Additionally, the gate leakage current of TFT with interlayer is slightly smaller than that of TFT without interlayer (not shown here), implying the gate dielectric with additional SiO_2 interlayer could block gate leakage better. The excellent device performance of the proposed TFT with interlayer may be attributed to the improved interface quality and modified grain boundaries (GBs) near the surface of poly-Si film. The interface trap states [12], mainly generated by the Si dangling bonds, have a wide energy distribution in the band gap. The thermal SiO_2 grown on the top of poly-Si film may greatly improve interface quality by generating less Si dangling bonds, decreasing the density of states over a wide energy range and therefore improving μ_{FE}, V_{th} and SS [13]. Also due to the improved interface quality, the interface trap-assisted tunneling [14] may be greatly alleviated, resulting in significant improvement in GIDL current. On the other hand, when oxidizing the poly-Si film, excess Si interstitials generated at and migrated from the oxidizing interface would modify the GBs at the surface of poly-Si film by facilitating the climb of intrinsic GB dislocations and therefore result in lower trap state density (N_t) [15] and improved μ_{FE}, V_{th} and SS [13]. The GB N_t could be estimated by using Proano and Levinson method [16], [17] at low source-drain voltage and

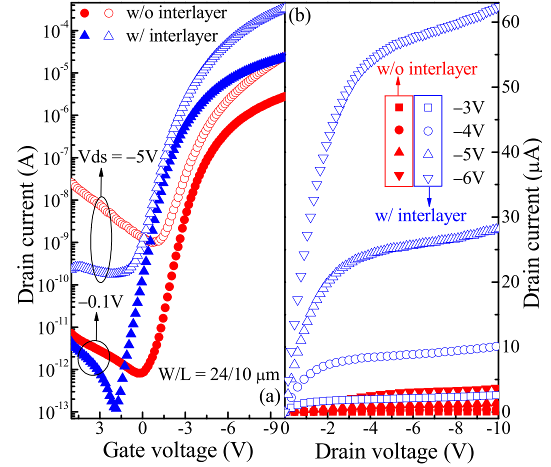

Fig. 2. Comparison of (a) transfer characteristics and (b) output characteristics between the proposed SPC TFTs with and without thermal SiO_2 interlayer.

TABLE I

PARAMETER COMPARISON FOR SPC TFTs WITH DIFFERENT DIELECTRICS AT $V_{ds} = -0.1$ V. THE VALUE FOR TFTs WITH OR WITHOUT INTERLAYER IS THE MEAN VALUE CALCULATED FROM 10 TFTs

Parameters	SiO_2 [6]	w/o interlayer	w/ interlayer
EOT (nm)	70	35.93	39.73
μ_{FE} (cm^2 Vs^{-1})	8.74	18.02	67.80
V_{th} (V)	−19.12	−5.18	−3.78
SS (V dec^{-1})	1.86	0.76	0.62
I_{on}/I_{off}	6.13×10^5	3.55×10^6	2.31×10^8
I_{on}/I_{off} (at V_{ds}=−5V)	2.93×10^5	2.74×10^4	1.87×10^6
GB N_t (cm^{-2})	−	5.52×10^{12}	4.98×10^{12}

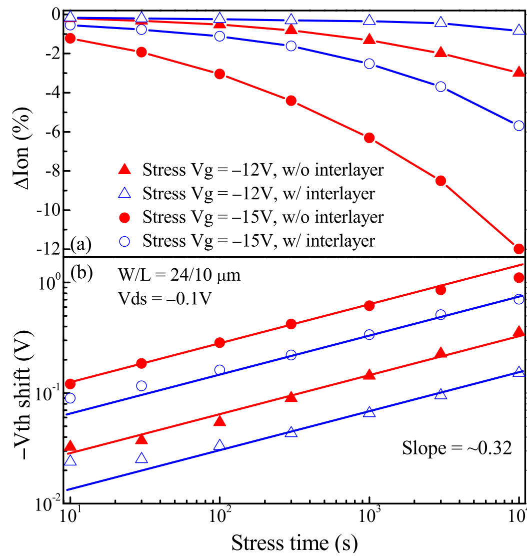

Fig. 3. (a) I_{on} degradation and (b) negative V_{th} shift as a function of stress time in the proposed SPC TFTs with/without interlayer under NBT stresses.

high gate bias. As shown in Table I, the GB N_t of TFT with and without interlayer are calculated as 4.98×10^{12} cm^{-2} and 5.52×10^{12} cm^{-2} respectively, implying the GBs is indeed improved when performing the oxidation of poly-Si film. Shown in Fig. 2(b) are output curves of TFTs with and without interlayer. Consistent to transfer curves, TFT with interlayer greatly enhances the I_{on}.

The instability of proposed SPC TFT with and without interlayer under NBT stress is also examined. Shown in Fig. 3(a) and (b) are I_{on} degradation and negative V_{th} shift as a function of stress time for TFTs with and without interlayer under NBTI degradation. For the NBT stress, a negative bias was applied to the gate electrode with source/drain grounded. As shown in Fig. 3, the degradation slope is about 0.32, consistent to previous report [18]. It can be observed that under the same NBT stress, the proposed TFT with interlayer exhibits much more reliable characteristics. The NBT stress [8], [18], which breaks the bonds at interface/GBs and generates dangling bonds, brings more interface/GB trap states and degenerates the device. Thus, the reliability test results reveal that the proposed TFT with interlayer possesses superior interface/GB quality.

IV. CONCLUSION

In this letter, a simple method is proposed to grow thermal SiO_2 during SPC process. By employing thermal SiO_2 interlayer between SPC poly-Si channel and Al_2O_3 gate dielectric, all the device parameters of TFT are improved due to the superior interface quality and modified GBs by excess Si interstitials. Furthermore, the proposed TFT with interlayer exhibits better reliability under NBT stress. The test results reveal that the proposed method and related TFT have great potential for SOP applications.

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