Characteristics of Elevated-Metal Metal-Oxide Thin-Film Transistors Based on Indium-Tin-Zinc Oxide

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***Abstract*— Based on the distinct effects of oxidizing thermal annealing on the properties of zinc oxide and indium-gallium-zinc oxide (IGZO) under covers of different gas-permeabilities, the elevated-metal metal-oxide (EMMO) thin-film transistor (TFT) architecture has been proposed and demonstrated using IGZO as the channel material. However, the speculation that the EMMO architecture is more generally applicable to semiconducting metal oxides other than IGZO has yet to be verified. Presently reported is an EMMO TFT with a modified structure employing indium-tin-zinc oxide as the channel material. The resulting TFT exhibited good performance metrics: a relatively higher field-effect mobility of 23.2 ± 0.8 cm^2/Vs, an ON/OFF current ratio of at least 3.1 × 10^{10}, a pseudo subthreshold slope of 165 ± 15 mV/decade, a width-normalized OFF-state current of at most 8.1 ×10^{-19}A/μm, and robust stability against gate-bias stress.**

***Index Terms*— Indium-tin-zinc oxide (ITZO), thin-film transistors (TFTs), low off-state current, elevated-metal.**

I. Introduction

DUE to their process requirements similar to the making of amorphous silicon thin-film transistor (TFT) and relatively higher field-effect mobility (μ_{FE}), metal-oxide (MO) TFTs are being deployed in the construction of active-matrix liquid-crystal displays (AMLCDs) and active-matrix organic light-emitting diode (AMOLED) displays [1]–[5]. Based on the distinct effects of oxidizing thermal annealing on the properties of MO semiconducting thin films under covers of different gas-permeability [6], the elevated-metal metal-oxide (EMMO) TFT architecture has been proposed [7].

Presently proposed is an alternative EMMO TFT structure (Fig. 1a) that looks deceptively similar to the conventional etch-stop (ES) TFT structure (Fig. 1b) but allows a reduction in the minimum channel length (L) from 3 λ to 1 λ, where λ is the minimum lithography feature size. This is made possible by the incorporation of conductive annealing-induced source/drain (S/D) regions in the EMMO TFT such that L is defined by the separation between the S/D electrodes (Fig. 1a), as in a back-channel etched TFT, rather the length of the etch-stop layer (Fig. 1b) in an ES TFT. The resulting small device foot-print immediately leads to an increase in the aperture ratio of an EMMO TFT driven sub-pixel (Fig. 1c) compared to that of an ES TFT driven sub-pixel (Fig. 1d) - assuming a channel width (W)-to-L ratio of 2.5, a design-rule of 2 μm and a 500ppi AMLCD.

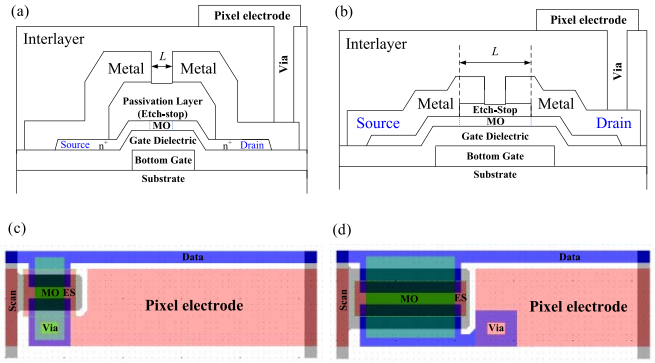

Fig. 1. The cross-sectional schematics of (a) an EMMO and (b) an ES TFT and the corresponding layouts of a 500-ppi AMLCD sub-pixel based on (c) an EMMO and (d) an ES TFT with a W-to-L ratio of 2.5 and a design-rule of 2 μm.

The EMMO architecture has been demonstrated using indium-gallium-zinc oxide (IGZO) as the channel material [7], with the resulting TFT exhibiting low parasitic S/D and contact resistance, low off-state current and good reliability against electrical stress [8].

Made viable by controlling the population of oxygen-related defects in the channel and S/D regions, the EMMO architecture has been speculated to be applicable to MOs other than IGZO [9]. Hitherto it has been difficult to realize EMMO TFT based on zinc oxide (ZnO) – in which annealing-induced conductivity was first reported, – hence the validity of the speculation has yet to be verified. Amorphous indium-tin-zinc oxide (ITZO) [10] is a material worthy of this investigation, because of the replacement of Ga by the more abundantly available tin (Sn) and reports of high $\mu_{FE} \sim 50$ cm^2/Vs [11]. TFTs with a μ_{FE} of at least 16 cm^2/Vs are needed to realize an 8k × 4k AMOLED display driven at 120 Hz [12]. This is higher than the typical ~ 10 cm^2/Vs offered by IGZO TFTs. Presently reported is the fabrication and characterization of EMMO TFTs based on a modified architecture using ITZO as the channel material.

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II. Experimental

The fabrication of an EMMO TFT (Fig. 1a) started with the sputter deposition and patterning of 120 nm-thick molybdenum (Mo) gate electrode on an oxidized n-type silicon substrate. The gate dielectric consisted of 50-nm thick silicon nitride (SiN_x) and 75-nm thick silicon oxide (SiO_y), formed using plasma-enhanced chemical vapor deposition (PECVD) with respective carrier gases of 40 sccm silane/40 sccm ammonia and 8 sccm silane/1400 sccm nitrous oxide; the temperature and pressure were 300 °C and 0.9 Torr. A 30 nm-thick ITZO active layer was deposited at room temperature by the co-sputtering of ZnO and ITZO in a radio-frequency magnetron sputtering machine at a process pressure of 3 mTorr in an atmosphere of 40% oxygen (O_2) and 60% argon. The molar ratio of the ITZO target was In_2O_3:SnO_2:ZnO = 35:35:30 and the base pressure was ~ 1 μTorr. The active layer was patterned using 1/2000 molar aqueous hydrofluoric acid solution, before a 300 nm-thick SiO_y passivation layer was deposited using the same PECVD process. Following a thermal treatment at 300 °C for 2 hrs in an O_2 atmosphere, contact holes were opened in an inductively coupled plasma etcher running a sulfur hexafluoride chemistry. The S/D electrodes were made of sputtered and patterned stacks of 50-nm thick Mo and 300-nm thick aluminum (Al). The overlap (Fig. 1a) between each end of the gate electrode and the corresponding S/D electrode was 4 μm. Finally, conductive S/D regions were formed using a thermal treatment at 400 °C in O_2 for 4 hrs. The TFTs were electrically characterized at room temperature using an Agilent 4156C semiconductor parameter analyzer.

III. Results and Discussion

As schematically shown in Figure 1a, the metal- and oxide-covered ITZO form the respective S/D and the channel regions of an EMMO TFT. The metal and oxide are respectively impermeable and permeable to O_2, the atmosphere in which the thermal treatment was performed. Plotted in Figure 2 is the dependence of the respective resistivity values on the thermal treatment time.

Starting with a value of 2.0 $\pm$0.4$\Omega\cdot$ cm for the as-fabricated ITZO, the resistivity of the metal-covered ITZO monotonically decreased with increasing treatment time and reached a low value of (2.20 $\pm$0.04) $\times 10^{-2}\Omega\cdot$ cm after 4 hrs of treatment; whereas the opposite behavior was observed for the oxide-covered ITZO, with the resistivity reaching a high value of (9.3 $\pm$1.4) $\times 10^{2}\Omega\cdot$ cm after the same treatment duration. Similar behavior has been reported for ZnO and IGZO [9], [13] and explained in terms of the formation and suppression of donor-defects in MO respectively under impermeable and permeable covers. Shown in the Inset is the transfer curves of EMMO ITZO TFTs with and without going through a thermal annealing process. The drain current (I_d) in the "on" state (on-current) of the former is clearly limited by high parasitic S/D resistance. With the annealing-induced generation of donor-defects in the ITZO underneath the impermeable S/D electrodes, conductive S/D regions are formed in the latter – resulting in significantly improved on-current.

Shown in Figure 3 is I_d *vs.* gate voltage (V_g) transfer characteristics of an EMMO TFT subjected to different drain bias (V_d). Hysteresis was negligible, as reflected by the excellent overlap of the transfer characteristics resulting from both forward and reverse V_g sweep at a rate of 1.5V/s, as indicated by the arrows in the figure. The I_d *vs.* V_d output characteristics

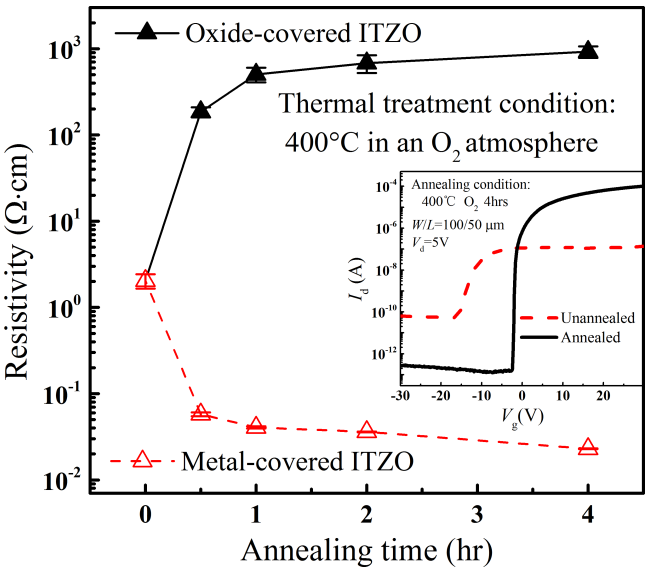

Fig. 2. The dependence of the resistivity values of metal- and oxide-covered ITZO on thermal treatment time. Shown in the Inset are the transfer characteristics of EMMO ITZO TFTs with and without going through a thermal annealing process.

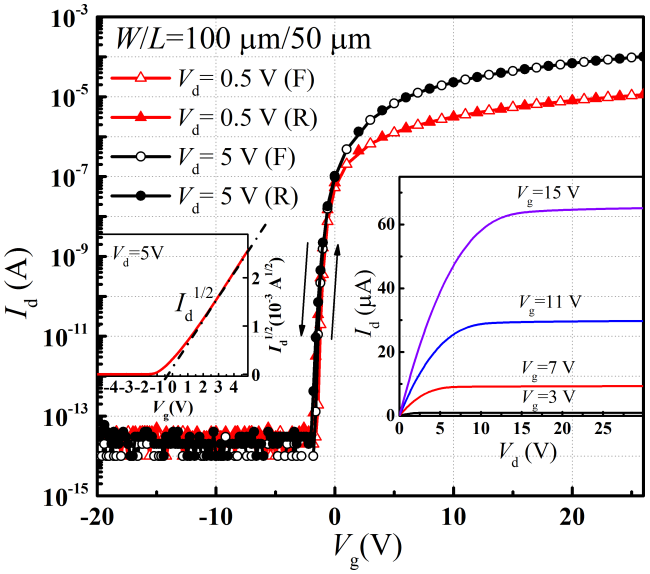

Fig. 3. The forward (F) and reverse (R) transfer characteristics of an EMMO ITZO TFT at V_d of 0.5 and 5 V. Shown in the Left Inset is $I_d^{1/2}$ versus V_g of the same TFT and in the Right Inset is the output characteristics of the same TFT at various V_g.

shown in the Inset reveal nice linearity at small V_d, indicating good ohmic contact between a conductive S/D region and a Mo/Al metal electrode.

A μ_{FE} ($\equiv Lg_m/WC_iV_d$) of 23.2$\pm$0.8 cm^2/Vs was extracted from the maximum trans-conductance (g_m) at a low V_d of 0.5 V, where C_i is the gate capacitance per unit area. An *SS* of 165 $\pm$ 15 mV/decade was extracted from the minimum value of $\partial \log I_d/\partial V_g$ when V_g is larger than the turn-ON voltage V_{on} ($\equiv V_g$ to induce an I_d of $L/W\times 10$ nA at $V_d = 5$ V) of -0.8 V. With the measurement of the off-state current limited by the noise level of $\sim 2.3\times 10^{-14}$ A, a lower bound of 3.1×10^{10} was estimated for the on/off current

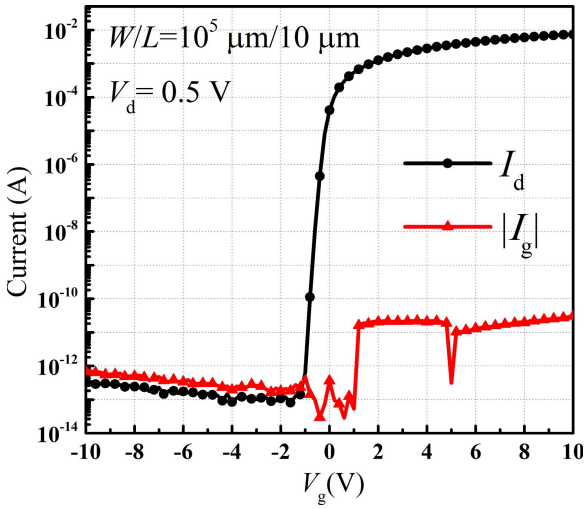

Fig. 4. The transfer characteristics of a wide EMMO ITZO TFT with W of $10^5\mu$m.

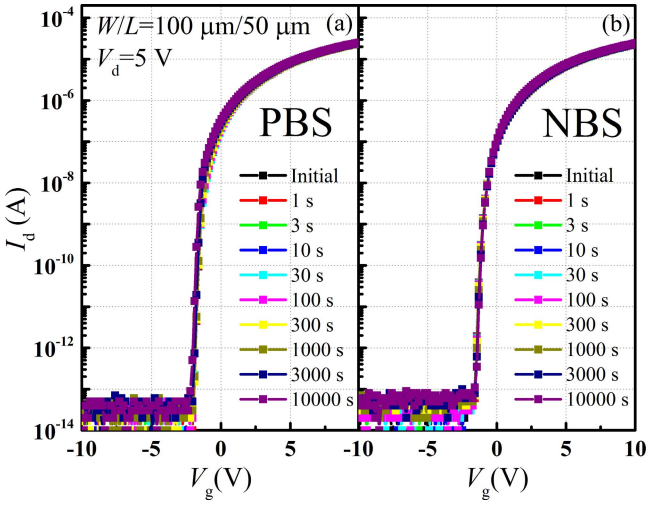

Fig. 5. The time evolution of the transfer characteristics of EMMO ITZO TFTs subjected to (a) PBS and (b) NBS with V_g of $V_{on}\pm20$ V.

ratio. For a more accurate estimation of the off-state leakage current, a TFT with a large W/L [14] of $10^5\mu$m /10 μm was fabricated and the corresponding transfer characteristic is shown in Figure 4. From the noise-limited off-state current of $\sim 8.1\times10^{-14}$A, a W-normalized off-state current of no larger than 8.1×10^{-19}A/μm was obtained.

The gate bias stress-induced instability of the EMMO TFT was characterized, with respective V_g of $V_{on}+20$ V and $V_{on}-20$ V for the positive and the negative bias stress (PBS/NBS). The evolution of the respective transfer characteristics with the stress time is shown in Figures 5a and 5b. Shifts in V_{on} of ~ -0.15 V for PBS and $\sim +0.15$ V for NBS were obtained after 10^4 s of stress. These are considered negligible as they are equal in magnitude to the V_g step of 0.15 V used during the measurement.

The quality of the oxidized ITZO, similar to that in the channel region, was characterized using X-ray photoelectron spectroscopy (XPS). Prior to the measurement, the top 5 nm of the samples were removed using *in situ* argon ion bombardment to eliminate surface contaminants such as dissociated O_2 or OH, adsorbed H_2O or O_2, and chemisorbed species such as $-CO_3$ [15]. O 1s spectra were obtained from un-annealed

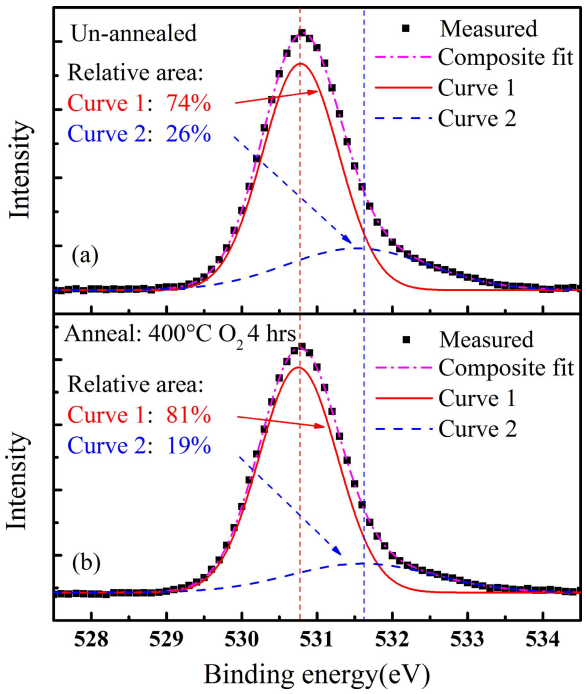

Fig. 6. XPS spectra of O 1s in (a) un-annealed ITZO and (b) ITZO annealed for 4 hrs at 400 °C in an O_2 atmosphere.

ITZO (Fig. 6a) and ITZO heated for 4 hrs in O_2 at 400°C (Fig. 6b).

Each spectrum was decomposed into two constituent components using Gaussian fitting, with the one centered at $\sim$ 530.8 eV labelled as "Curve 1" and the other centered at $\sim$ 531.6 eV labelled as "Curve 2". These correspond respectively to O^{2-} ions bonding to neighboring In^{3+}, Sn^{4+} and Zn^{2+} in stoichiometric ITZO [16], [17] and oxygen atoms in the vicinity of oxygen vacancies [18], [19]. Normalized by the total area of each composite spectrum, the relative area of the Curve 2 component is expressed as a percentage and taken to be a measure of the population of oxygen vacancies [20].

Compared with the relative area of 26% for Curve 2 of the un-annealed film, the relative area of Curve 2 of the thermally treated sample decreased to 19%, indicating a reduction in the population of oxygen vacancy defects and an improvement in the electrical quality of the film. This is consistent with the negligible hysteresis (Fig. 3), the low off-state current (Fig. 4) and the good reliability against gate-bias stress (Fig. 5).

IV. Conclusion

EMMO TFTs with ITZO as the channel material have been realized and characterized. Good performance metrics were obtained: such as transfer characteristics free of hysteresis, high on/off current ratio and a low width-normalized off-state leakage current of at most 8.1×10^{-19}A /μm. Stability against gate-bias stress has also been demonstrated.

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