Preliminary Program

<table>
<tr><th colspan="3">2016/10/26 Wednesday Day 1 (1/3)</th></tr>
<tr><td colspan="2">Tutorials (No. 5 Meeting Room)</td><td rowspan="9">Registration (09:00 – 18:00)</td></tr>
<tr><td>9:30 – 10:30</td><td>Jin Jang Kyung Hee University, Korea
“Device and Process Technologies of Oxide and LTPS TFTs for Display Manufacturing”</td></tr>
<tr><td>10:30 – 11:30</td><td>Arokia Nathan University of Cambridge, UK
“Oxide Semiconductor TFT Technology for Circuits and Systems”</td></tr>
<tr><td colspan="2">Lunch</td></tr>
<tr><td>13:30 – 14:30</td><td>Tse Nga (Tina) Ng University of California San Diego, USA
“Printed Organic TFT Sensor Tags”</td></tr>
<tr><td>14:30 – 15:30</td><td>Feng Yan The Hong Kong Polytechnic University, China
"Biosensors based on Thin Film Transistors"</td></tr>
<tr><td>15:30 – 16:00</td><td>Break</td></tr>
<tr><td>16:00 – 18:00</td><td>Panel Discussion organized by IEEE EDS Organic Electronics Committee
“Opportunities and Challenges of Organic Thin-Film Transistors”</td></tr>
</table>

2016/10/27 Thursday Day 2 (2/3)			
08:45 – 09:00	**Opening** (Gingko Hall，银杏大厅)		
09:00 – 10:30	**Plenary Session 1** (Gingko Hall，银杏大厅)		
09:00 - 09:30	**Samar Saha** President of IEEE Electron Device Society “ IEEE Electron Devices Society: Mission and Technical Activities”		
09:30 - 10:00	**Arokia Nathan** University of Cambridge, UK “Design Tools for TFT Circuits and Systems”		
10:00 - 10:30	**Kwang-Ting (Tim) Cheng** Hong Kong University of Science and Technology, China "Robust Design and Reliability Simulation for TFT Circuits"		
Coffee Break			
10:50 – 12:15	**Session 1: Devices and Circuits for Displays** (Gingko Hall)	**10:50 – 12:15**	**Session 2: High Performance TFTs** (No. 5 Meeting Room)
10:50 – 11:10 Invited	**Yanzhao Li** BOE, China “TFT Recent Progress and Its Applications”	10:50 – 11:10 Invited	**Lei Liao** Wuhan University, China “Rational Hydrogenation for Enhanced Mobility and High Reliability on ZnO-based Thin Film Transistors: from Simulation to Experiment”
11:10 – 11:30 Invited	**Lei Wang** Guangzhou New Vision Optoelectronic Tech., China “Progress on Flexible & Printed OLED Displays and their TFT Backplane Technology”	11:10 – 11:30 Invited	**Yong-Young Noh** Dongguk University, Korea "Development of High Performance Printed Ambipolar Polymer and Carbon Nanotube Complementary Integrated Circuits for Flexible Electronics"
11:30 – 11:45	**Siming Hu** Kunshan New Flat Panel Display Tech. Center, China “A New CMOS Pixel Compensation Circuit for AMOLED Display”	11:30 – 11:45	**Shubin Pi** Fudan University, China Investigation of Nitrogen Doping and Double Channel Layers for the Indium Tungsten Oxide Thin Film Transistors
11:45 – 12:00	**Wenjiang Liu** Shanghai Jiao Tong University, China “Current Feedback Driving with Dynamic Supply Voltage Scaling for Low Power AMOLED Displays”	11:45 – 12:00	**Changdong Chen** Sun Yat-Sen University , China “Ultra-High Mobility Thin-film Transistors with MOCVD Growth In_2O_3”
12:00 –	**Linlin Fang** Northeastern University,	12:00 – 12:15	**Seungpyo Hong** Kyung Hee University, Korea

12:15	China “Carbon Nanotube Thin-film Transistors and Driving Circuits for Flexible Display Application”		“Reduction of Leakage Current by Wet Annealing on BLA Polycrystalline Silicon Thin-Film Transistor”
Lunch			
14:00 – 15:10	**Session 3: TFT New Applications (Gingko Hall)**	**14:00 – 15:10**	**Session 4: Printed TFTs (No. 5 Meeting Room)**
14:00 – 14:20 Invited	**Qing Wan** Nanjing University, China “Oxide-based Electric-Double-Layer Thin-Film Transistors For Neuromorphic Systems”	14:00 – 14:20 Invited	**Mario Caironi** CNST of IIT, Italy "Enhancing the Speed of Printed and Direct-written Polymer Transistors"
14:20 – 14:40 Invited	**Kai Wang** Sun Yat-Sen University, China “Beyond Display: Emerging Applications of Thin-Film Transistors”	14:20 – 14:40 Invited	**Linfeng Lan** South China University of Technology, China “Printed Short-channel Thin-film Transistors”
14:40 – 14:55	**Vahid Keshmiri** Linköping University, Sweden “The Applications of OECTs in Supercapacitor Balancing Circuits”	14:40 – 14:55	**Jianwen Zhao** SINANO, CAS, China “Printed Thin-film Transistors and Circuits Based on Sorted Semiconducting Single-walled Carbon Nanotubes”
14:55 – 15:10	**Hantao He** Sun Yat-sen University, China “A Fluorescence Detector for Rapid On-Chip Detection of Amniotic Fluid Embolism Biomarker Based on Dual-Gate Photosensitive Thin-Film Transistor”	14:55 – 15:10	**Guixia Jiang** Qingdao University, China “Solution-Processed High-k Magnesium Oxide Dielectric for n-Type In_2O_3 and p-Type NiO Thin Film Transistors”
Coffee Break			
15:30 – 16:55	**Session 5: TCAD and Compact Modeling (Gingko Hall)**	**15:30 – 16:55**	**Session 6: Device Stabilities (No. 5 Meeting Room)**
15:30 – 15:50 Invited	**Ahmed Nejim** Silvaco, UK "TCAD for Compact Model Development? Get Real!"	15:30 – 15:50 Invited	**Shengdong Zhang** Peking University, China “Oxygen Adsorption Effects of Metal Oxide Thin Film Transistors”
15:50 – 16:10 Invited	**Radu Sporea** University of Surrey, UK "TCAD and Circuit Simulation of Thermal Effects in Source-gated Transistors"	15:50 – 16:10 Invited	**Hongtao Cao** NIMTE, CAS, China “Investigation on the Stability of Ambipolar SnO TFTs”
16:10 – 16:25	**Quan Chen** The University of Hong Kong, China “Artificial Neural Network Compact Model for TFTs”	16:10 – 16:25	**Wei Tang** Shanghai Jiao Tong University, China “Improved Bias Stress Stability for Low-voltage Polymer OTFTs with Low-k/High-k Bilayer Gate Dielectric”
16:25 – 16:40	**Guangwei Xu** Institute of Microelectronics, CAS, China	16:25 – 16:40	**Gongtan Li** Sun Yat-Sen University, China

	“The Description of Pinch-off Point for Short Channel Organic Thin Film Transistors”		“Nitrogen Doping Amorphous InGaZnO Thin Film Transistors for Highly Stable Operation Under Gate Bias and Light Stressing”
16:40 – 16:55	**Jielin Fang** Jinan University, China “Physical Modeling of AOS TFTs Based on Symmetric Quadrature Method Considering Degenerate Regime”	16:40 – 16:55	**Jianeng Xu** Shanghai Jiao Tong University, China “Ambient Effects on the Light Illumination Stability of Amorphous InGaZnO Thin Film Transistors”
17:00-18:30	**Poster Session (Gingko Hall)**		
18:40	**Banquet**		

<table>
<tr><th colspan="4">2016/10/28 Friday Day 3 (3/3)</th></tr>
<tr><td>9:00 – 10:30</td><td colspan="3">Plenary Session 2 (Gingko Hall)</td></tr>
<tr><td>09:00 - 09:30</td><td colspan="3">Benjamin Iñiguez, Universitat Rovirai Virgili, Spain
"Recent Progress in TFT Compact Modeling and Parameter Extraction Techniques"</td></tr>
<tr><td>09:30 - 10:00</td><td colspan="3">Yunqi Liu Institute of Chemistry, Chinese Academy of Sciences, China
"High Performance Organic Field-Effect Transistors and Circuits"</td></tr>
<tr><td>10:00 - 10:30</td><td colspan="3">Jamal Deen McMaster University, Canada
"Compact Modeling of Organic/Polymeric Thin Film Transistors - Past, Present and Future"</td></tr>
<tr><td colspan="4">Coffee Break</td></tr>
<tr><td>10:50 – 12:15</td><td>Session 7: Circuit Design (Gingko Hall)</td><td>10:50 – 12:20</td><td>Session 8: Simulation & Characterization (No. 5 Meeting Room)</td></tr>
<tr><td>10:50 – 11:10
Invited</td><td>Jordi Carrabina Bordoll Univ Autonoma de Barcelona, Spain
"Process Design Kit and EDA Tools for Organic/Printed Electronics"</td><td>10:50 – 11:10
Invited</td><td>Chao Jiang The National Center for Nanoscience and Tech., China
“Vertical Charge Transport via Small Polaron Hopping within Lamellar Organic Single Crystal”</td></tr>
<tr><td>11:10 – 11:30
Invited</td><td>Byong-Deok Choi Hanyang University, Korea
"Oxide-TFT Circuit Design for High-Reliability Flexible Electronics"</td><td>11:10 – 11:30
Invited</td><td>Sungsik Lee University of Cambridge, UK
"Threshold Voltage and Conduction Mechanisms in Disordered Semiconductor-based Thin Film Transistors"</td></tr>
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“Noise Margin Analysis for Pseudo-CMOS Circuits”</td><td>11:30 – 11:50
Invited</td><td>Di Geng Kyung Hee University, Korea
“Mobility and V_{th} Extraction by Time-of-flight Analysis for a-IGZO TFTs”</td></tr>
<tr><td>11:45 – 12:00</td><td>Manuel Llamas Universitat Autònoma de Barcelona, Spain
“Technology Independent Yield-Aware Place & Route Strategy for Printed Electronics Gate Array Circuits”</td><td>11:50 – 12:05</td><td>Zhiheng Han Institute of Microelectronics, CAS, China
“Surface Potential Measurement on Contact Resistance of a-IGZO TFTs by Kelvin Probe Force Microscopy”</td></tr>
<tr><td>12:00 – 12:15</td><td>Huimin Li Sun Yat-sen University, China
“Design Methodology for a Fingerprint Sensor-Integrated Display Pixel and Array based on Dual-Gate a-Si:H Photosensitive TFT”</td><td>12:05 – 12:20</td><td>Michiaki Sakamoto Japan Display Inc., Japan
“Simulation for Unidirectional Ion Flow in TFT-LCDs Induced by AC-Pixel-Driving Signals”</td></tr>
<tr><td colspan="4">Lunch</td></tr>
<tr><td>14:00 – 15:10</td><td>Session 9: New Material TFTs (Gingko Hall)</td><td>14:00 –</td><td>Session 10: Organic TFTs (No. 5 Meeting Room)</td></tr>
</table>

		15:10	
14:00 – 14:20 Invited	**Xuelei Liang** Peking University，China "Carbon Nanotube Thin Film Transistors for Display Technology"	14:00 – 14:20 Invited	**Simon Ogier** Neudrive, UK "High Performance Flexible OTFT Materials and Processes for Display, Logic and Sensor Applications"
14:20 – 14:40 Invited	**Fukai Shan** Qingdao University, China "The Fully Solution-processed p-type Metal Oxide Thin Film and its Integration for Thin Film Transistors"	14:20 – 14:40 Invited	**Chuan Liu** Sun Yat-sen University, China "On the Controversy of Carrier Mobility in Organic TFTs"
14:40 – 14:55	**Yuzhi Li** South China University of Technology, China "Low Temperature, Stable Thin-film Transistors based on Photo-patternable Solution-processed InOx:Li Semiconductors"	14:40 – 14:55	**Longzhen Qiu** Hefei University of Technology, China "Polymer Brush Modified Surface for High-performance Inkjet-printed Organic Thin-film Transistors"
14:55 – 15:10	**Lingyan Liang** NIMTE, CAS, China "The Physical Properties of Zn-Sn-N Thin Films and their TFT Application"	14:55 – 15:10	**Jiaqing Zhao** Shanghai Jiao Tong University, China "Low Voltage Organic Thin-film Transistor with Reduced Sub-gap DOS for Power Efficient Logic Circuits"
		Coffee Break	
15:30-16:55	**Session 11: New Circuit Technologies (Gingko Hall)**	**15:30-16:55**	**Session 12: Flexible TFTs (No. 5 Meeting Room)**
15:30 – 15:50 Invited	**Ta-Ya Chu** National Research Council, Canada "Development of Printed Logic Circuits"	15:30 – 15:50 Invited	**Xifeng Li** Shanghai University, China High Stability of Low Temperature and Flexible IGZO TFT by Plasma Treatment
15:50 – 16:10 Invited	**Deyu Tu** Linköping University, Sweden "Organic Power Electronics: AC-DC Conversion with High-Voltage Organic Thin-film Transistors"	15:50 – 16:10 Invited	**Dong-Ming Sun** Institute of Metal Research, CAS, China "Scale-up Fabrication of Single Wall carbon Nanotube Thin Film and its Application in Flexible Thin-film Transistors"
16:10 – 16:25	**Nan Yang** Kunshan New Flat Panel Display Tech Center, China "A New p-type Shift Register with Detection Function for Flexible Display"	16:10 – 16:25	**Kun Hu** Kunshan New Flat Panel Display Tech Center, China "Failure Mechanism of TFT Devices on Flexible Substrate by Cyclic Bending Test"
16:25 – 16:40	**Zheyu Liu** Tsinghua University, Beijing, China "Computable Flexible Electronics: Circuits Exploring for Image	16:25 – 16:40	**Younwoo Choe** Kyung Hee University, Korea "Bendable Corbino a-IGZO TFTs"

	Filtering Accelerator with OTFT"		
16:40 – 16:55	**Ahmed Rasheed** Sun Yat-Sen University, China "Heart Rate/Impulse Monitoring Using Autonomous PVDF-Integrated Dual-Gate Thin-Film Transistor"	16:40 – 16:55	**Peng Xiao** South China University of Technology, China "High-mobility Flexible Thin-film Transistors with Zirconium-doped Indium Oxide Channel Layer"
17:10-17:40 **(Gingko Hall)**	**Award Session** **Announcement of 2018 CAD-TFT** **Closing remarks**		

Abstract for Tutorials

No.	Title	Author	Affiliation
T01	Device and Process Technologies of Oxide and LTPS TFTs for Display Manufacturing	Jin Jang	Kyung Hee University, Korea
T02	Oxide Semiconductor TFT Technology for Circuits and Systems	Arokia Nathan	University of Cambridge, UK
T03	Printed Organic TFT Sensor Tags	Tse Nga (Tina) Ng	University of California San Diego, USA
T04	Biosensors based on Thin Film Transistors	Feng Yan	Hong Kong Polytechnic University, China

Abstract for Plenary Presentations

No.	Title	Author	Affiliation
PI01	IEEE Electron Devices Society: Mission and Technical Activities	Samar Saha	President of IEEE Electron Device Society
PI02	Design Tools for TFT Circuits and Systems	Arokia Nathan	University of Cambridge, UK
PI03	Robust Design and Reliability Simulation for TFT Circuits	Kwang-Ting (Tim) Cheng	Hong Kong University of Science and Technology, China
PI04	Recent Progress in TFT Compact Modeling and Parameter Extraction Techniques	Benjamin Iñiguez	Universitat Rovirai Virgili, Spain
PI05	High Performance Organic Field-Effect Transistors and Circuits	Yunqi Liu	Institute of Chemistry, Chinese Academy of Sciences, China
PI06	Compact Modeling of Organic/Polymeric Thin Film Transistors - Past, Present and Future	M. Jamal Deen	McMaster University, Canada

Abstract for Invited Presentations

No.	Title	Topic	Author	Affiliation
INV1-1	TFT Recent Progress and Its Applications	**Devices and Circuits for Displays**	Yanzhao Li	BOE, China
INV1-2	Progress on Flexible & Printed OLED Displays and their TFT Backplane Technology		Lei Wang	Guangzhou New Vision Optoelectronic Tech., China
INV2-1	Rational Hydrogenation for Enhanced Mobility and High Reliability on ZnO-based Thin Film Transistors: from Simulation to Experiment	**High Performance TFTs**	Lei Liao	Wuhan University, China
INV2-2	Development of High Performance Printed Ambipolar Polymer and Carbon Nanotube Complementary Integrated Circuits for Flexible Electronics		Yong-Young Noh	Dongguk University, Korea

INV3-1	Oxide-based Electric-Double-Layer Thin-Film Transistors For Neuromorphic Systems	TFT New Applications	Qing Wan	Nanjing University, China
INV3-2	Beyond Display: Emerging Applications of Thin-Film Transistors		Kai Wang	Sun Yat-Sen University, China
INV4-1	Enhancing the Speed of Printed and Direct-written Polymer Transistors	Printed TFTs	Mario Caironi	CNST of IIT, Italy
INV4-2	Printed Short-channel Thin-film Transistors		Linfeng Lan	South China University of Technology, China
INV5-1	TCAD for Compact Model Development? Get Real!	TCAD and Compact Modeling	Ahmed Nejim	Silvaco, UK
INV5-2	TCAD and Circuit Simulation of Thermal Effects in Source-gated Transistors		Radu Sporea	University of Surrey, UK
INV6-1	Oxygen Adsorption Effects of Metal Oxide Thin Film Transistors	Device Stabilities	Shengdong Zhang	Peking University, China
INV6-2	Investigation on the Stability of Ambipolar SnO TFTs		Hongtao Cao	NIMTE, CAS, China
INV7-1	Process Design Kit and EDA Tools for Organic/Printed Electronics	Circuit Design	Jordi Carrabina Bordoll	Univ Autonoma de Barcelona, Spain
INV7-2	Oxide-TFT Circuit Design for High-Reliability Flexible Electronics		Byong-Deok Choi	Hanyang University, Korea
INV8-1	Vertical Charge Transport via Small Polaron Hopping within Lamellar Organic Single Crystal	Simulation & Characterization	Chao Jiang	National Center for Nanoscience and Tech., China

INV8-2	Threshold Voltage and Conduction Mechanisms in Disordered Semiconductor-based Thin Film Transistors		Sungsik Lee	University of Cambridge, UK
INV8-3	Mobility and V_{th} Extraction by Time-of-flight Analysis for a-IGZO TFTs		Di Geng	Kyung Hee University, Korea
INV9-1	Carbon Nanotube Thin Film Transistors for Display Technology	**New Material TFTs**	Xuelei Liang	Peking University, China
INV9-2	The Fully Solution-processed p-type Metal Oxide Thin Film and its Integration for Thin Film Transistors		Fukai Shan	Qingdao University, China
INV10-1	High Performance Flexible OTFT Materials and Processes for Display, Logic and Sensor Applications	**Organic TFTs**	Simon Ogier	NeuDrive Limited, Biohub, Macclesfield, United Kingdom
INV10-2	On the Controversy of Carrier Mobility in Organic TFTs		Chuan Liu	Sun Yat-sen University, China
INV11-1	Development of Printed Logic Circuits	**New Circuit Technologies**	Ta-Ya Chu	National Research Council, Canada
INV11-2	Organic Power Electronics: AC-DC Conversion with High-Voltage Organic Thin-film Transistors		Deyu Tu	Linköping University, Sweden
INV12-1	High Stability of Low Temperature and Flexible IGZO TFT by Plasma Treatment	**Flexible TFTs**	Xifeng Li	Shanghai University, China
INV12-2	Scale-up Fabrication of Single Wall carbon Nanotube Thin Film and its Application in Flexible Thin-film Transistors		Dong-Ming Sun	Institute of Metal Research, CAS, China

Abstract for Oral Presentations

No.	Title	Topic	Author	Affiliation
O1-01	Withdrawn	**Devices and Circuits for Displays**		
O1-02	Current Feedback Driving with Dynamic Supply Voltage Scaling for Low Power AMOLED Displays		Wenjiang Liu	Shanghai Jiao Tong University, China
O1-03	Carbon Nanotube Thin-film Transistors and Driving Circuits for Flexible Display Application		Linlin Fang	Northeastern University, China
O2-01	Investigation of Nitrogen Doping and Double Channel Layers for the Indium Tungsten Oxide Thin Film Transistors	**High Performance TFTs**	Shubin Pi	Fudan University, China
O2-02	Ultra-High Mobility Thin-film Transistors with MOCVD Growth In_2O_3		Yanli Pei	Sun Yat-Sen University , China
O2-03	Reduction of Leakage Current by Wet Annealing on BLA Polycrystalline Silicon Thin-Film Transistor		Seungpyo Hong	Kyung Hee University, Korea
O3-01	The Applications of OECTs in Supercapacitor Balancing Circuits	**TFT New Applications**	Vahid Keshmiri	Linköping University, Sweden
O3-02	A Fluorescence Detector for Rapid On-Chip Detection of Amniotic Fluid Embolism Biomarker Based on Dual-Gate Photosensitive Thin-Film Transistor		Hantao He	Sun Yat-sen University, China

O4-01	Printed Thin-film Transistors and Circuits Based on Sorted Semiconducting Single-walled Carbon Nanotubes	**Printed TFTs**	Jianwen Zhao	SINANO, CAS, China
O4-02	Solution-Processed High-k Magnesium Oxide Dielectric for n-Type In_2O_3 and p-Type NiO Thin Film Transistors		Guixia Jiang	Qingdao University, China
O5-01	Artificial Neural Network Compact Model for TFTs	**TCAD and Compact Modeling**	Quan Chen	The University of Hong Kong, China
O5-02	The Description of Pinch-off Point for Short Channel Organic Thin Film Transistors		Guangwei Xu	Institute of Microelectronics, CAS, China
O5-03	Physical Modeling of AOS TFTs Based on Symmetric Quadrature Method Considering Degenerate Regime		Jielin Fang	Jinan University, China
O6-01	Improved Bias Stress Stability for Low-voltage Polymer OTFTs with Low-k/High-k Bilayer Gate Dielectric	**Device Stabilities**	Wei Tang	Shanghai Jiao Tong University, China
O6-02	Nitrogen Doping Amorphous InGaZnO Thin Film Transistors for Highly Stable Operation Under Gate Bias and Light Stressing		Gongtan Li	Sun Yat-Sen University, China
O6-03	Ambient Effects on the Light Illumination Stability of Amorphous InGaZnO Thin Film Transistors		Jianeng Xu	Shanghai Jiao Tong University, China
O7-01	Noise Margin Analysis for Pseudo-CMOS Circuits	**Circuit Design**	Qinghang Zhao	Tsinghua University, China,
O7-02	Technology Independent Yield-Aware Place & Route Strategy for Printed Electronics Gate Array Circuits		Manuel Llamas	Universitat Autònoma de Barcelona, Spain
O7-03	Design Methodology for a Fingerprint Sensor-Integrated Display Pixel and Array based on Dual-Gate a-Si:H		Huimin Li	Sun Yat-sen University, China

	Photosensitive TFT			
O8-01	Surface Potential Measurement on Contact Resistance of a-IGZO TFTs by Kelvin Probe Force Microscopy	**Simulation & Characterization**	Zhiheng Han	Institute of Microelectronics, CAS, China
O8-02	Simulation for Unidirectional Ion Flow in TFT-LCDs Induced by AC-Pixel-Driving Signals		Michiaki Sakamoto	Japan Display Inc., Japan
O9-01	Low Temperature, Stable Thin-film Transistors based on Photo-patternable Solution-processed InOx:Li Semiconductors	**New Material TFTs**	Yuzhi Li	South China University of Technology, China
O9-02	The Physical Properties of Zn-Sn-N Thin Films and their TFT Application		Lingyan Liang	NIMTE, CAS, China
O10-01	Polymer Brush Modified Surface for High-performance Inkjet-printed Organic Thin-film Transistors	**Organic TFTs**	Longzhen Qiu	Hefei University of Technology, China
O10-02	Low Voltage Organic Thin-film Transistor with Reduced Sub-gap DOS for Power Efficient Logic Circuits		Jiaqing Zhao	Shanghai Jiao Tong University, China
O11-01	A New p-type Shift Register with Detection Function for Flexible Display	**New Circuit Technologies**	Nan Yang	Kunshan New Flat Panel Display Tech Center, China
O11-02	Computable Flexible Electronics: Circuits Exploring for Image Filtering Accelerator with OTFT		Zheyu Liu	Tsinghua University, Beijing, China
O11-03	Heart Rate/Impulse Monitoring Using Autonomous PVDF-Integrated Dual-Gate Thin-Film Transistor		Ahmed Rasheed	Sun Yat-Sen University, China
O12-01	Failure Mechanism of TFT Devices on Flexible Substrate by	**Flexible TFTs**	Kun Hu	Kunshan New Flat Panel

	Cyclic Bending Test			Display Tech Center, China
O12-02	Bendable Corbino a-IGZO TFTs		Younwoo Choe	Kyung Hee University, Korea
O12-03	High-mobility Flexible Thin-film Transistors with Zirconium-doped Indium Oxide Channel Layer		Peng Xiao	South China University of Technology, China

Abstract for Poster Presentations

No.	Title	Author	Affiliation
P001	Organic-inorganic Hybrid Ambipolar Field-effect Transistor with a Cytop interlayer	Sheng Sun	South China University of Technology, China
P002	Contact Length Optimization in Organic Thin-Film Transistors	Shiwei Wu	Xidian University, China
P003	Charge trapping performance based in Zr0.5Hf0.5O2 for nonvolatile memory	Xiaobing Yan	Hebei University, China
P004	A Physical Model for Double Gate Amorphous InGaZnO Thin Film Transistors Based on Multiple Trapping and Release Mechanism	Guanhua Yang	Institute of Microelectronics, CAS, China
P005	Three-Dimensional Fin-Shape Dual-Gate Photosenstive a-Si:H Thin-Film Transistor for Low Dose X-Ray Imaging	Hai Ou	Sun Yat-sen University, China
P006	Subthreshold Operation of PVDF-Integrated Dual-Gate Thin-Film Transistor for Tactice Sensing	Weiwei Li	Sun Yat-sen University, China
P007	Low voltage organic TFTs based on higk-k/low-k dielectrics	Qiutan Ke	Sun Yat-sen University, China
P008	Solution Combustion Synthesis of Alumina Gate Dielectric using Hydrogen Peroxide/Water Solvent	Bo Liu	Sun Yat-sen University, China
P009	Effects of active layer thickness and annealing temperature of	Jin Cheng	Beijing Institute of Technology,

	solution-processed InMgZnO thin film transistors		China
P010	Laser annealing effects on the performance of InTiZnO thin film transistors	You Meng	Qingdao University, China
P011	Low-temperature, Nontoxic water-induced high-k zirconium oxide dielectric for fully-solution processed oxide thin-film transistors	Chundan Zhu	Qingdao University, China
P012	Solution-Processed Organic Field-effect Transistors with High Mobility and Excellent Uniformity	Yukun Huang	Shanghai Jiao Tong University, China
P013	a-IGZO Thin Film Transistors with Offset Structure for Field Emitter Array Application	Xiaojie Li	Sun Yat-sen University, China
P014	Simulation and study of Double-Material Gate TFT in order to reduce sub-threshold swing	Atefeh Rahmaninejad	Shahid Rajaee Teacher Training University, iran
P015	Temperature Dependent Gate Bias Stress Effect in Dioctylbenzothieno[2,3-b]benzothiophene (C8BTBT) Based Thin Film Transistor	Jiawei Wang	National Center for Nanoscience and Technology, China
P016	Field-effect Electroluminescence Spectra of Reverse-biased PN Junctions in Silicon TFT Device for Microdisplay	Zhengfei Ma	niversity of Electronic Science and Technology of China, China
P017	Flexible Thin-film Transistors Fabricated on Plastic Substrate at Low Temperature	Huijin Li	Peking University,China
P018	Hybrid-Phase Microstructure in InSnZnO Thin Film and Its Application to High-Performance TFT	Rongsheng Chen	South China University of Technology, China
P019	Flexible Transparent Field-Effect Diodes Fabricated at Low-Temperature with All Oxide Materials	Yonghui Zhang	Institute of Physics, CAS, China
P020	A Novel Three-Terminal UV PD on Barrier-Modulated Triple-Layer Architecture	Daqian Ye	Institute of Physics, CAS, China

Device and Process Technologies of Oxide and LTPS TFTs for Display Manufacturing

Jin Jang
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***Abstract*— I will review the device structure, process and performance of LTPS and oxide TFTs. Excimer laser annealing of a-Si and TFT structure for LTPS TFTs will be discussed to understand AMOLED backplane design. The device structure and performance of oxide TFTs will be also explained to understand the conditions for high performance oxide TFT with excellent stability. In addition the bulk accumulation oxide TFTs studied in our lab will be discussed together with oxide TFTs on plastic substrate.**

***Keywords*—Oxide TFT, LTPS TFT, Bulk accumulation, TFT circuits**

I. Introduction

P-channel LTPS TFTs are being used for manufacturing of AMOLED for smart phones and a-IGZO TFT are for AMOLED TV. Excimer laser annealing of a-Si is widely used for LTPS on glass and PI substrates with grain size of less than 400nm. Multi-shots over 10 are used to improve the quality of grains and the uniformity of grain size. On the other hand, back-channel etched (BCE) and coplanar a-IGZO TFTs are used for LCD and OLED backplanes respectively. The performance and stability of a-IGZO TFTs will be explained on the basis of device physics and material properties.

II. Oxide TFTs

A. Device structures

Etch stopper, back-channel etched (BCE), coplanar and dual gate structure are being studied for oxide TFTs. I will discuss the issues for these structure in term of stability and high drain currents. ES TFT can be used for high quality oxide semiconductor in TFT, BCE for less mask oxide TFT process and coplanar is for high speed circuits. However, the process issues for these TFTs are very different.

B. High perofrmance a-IGZO TFTs with excellent stability

Bulk accumulation can be possible when the carrier concentration is almost uniformly distributed in the channel region including front and back interface regions. This is especially important because the mobility in oxide semiconductor increases with carrier concentration. We demonstrated the advantages of BA a-IGZO TFTs such as 3 to 5 times of drain currents, excellent Vth uniformity and excellent bias stability [1-9]. The device physics under the BA TFTs will be explained. Coplanar oxide TFTs will be also discussed because of its advantage of low parasitic capacitance and thus high speed gate drivers. The TFT circuits such as ring oscillator and shift resistor will be touched.

We developed non-detach technology of plastic TFTs using CNT/GO buffer layer [10] and also TFTs on neutral plane to have rollable TFTs at the radius of 0.26mm [11].

III. LTPS

LTPS is used for high resolution displays such as smart phone AMLCD with FFS mode and for AMOLED with top emission. Recently flexible AMOLED is a hot issue because of recent display product trend of mobile applications. I will review the conventional ELA process and issues for ELA TFTs. The device structures for AMOLED will be also explained. In order to reduce the production cost we are studying blue laser annealing of a-Si to replace current ELA LTPS [12]. The field-effect mobility of >100cm^2/Vs was achieved.

Acknowledgment

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T02

Oxide Semiconductor TFT Technology for Circuits and Systems

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Oxide semiconductors are known for their optical transparency and high electron mobility even when processed at room temperature, making them a promising candidate for the next-generation thin film transistor (TFT) technology. Compared to existing well-established TFT technologies, the oxide transistor shows superiority in terms of process simplicity and cost, and stable device behaviour in the dark. While its non-uniformity over large areas is comparable to that of thin film silicon transistors, its photo-instability at low wavelengths can be an issue due to persistence in photoconductivity. This tutorial will review the mechanisms underlying light sensitivity in oxide transistors. Although this class of materials is optically transparent, the presence of oxygen deficiency defects, such as vacancies and interstitials located at gap states, gives rise to absorption of blue and green photons due to their ionization. In particular, the oxygen defects remain ionized even after illuminating, leading to persistent photoconductivity (PPC). This can limit the frame-rate of pixelated arrays for imaging and displays. However, despite material weaknesses, considerable progress has been made in designing oxide-based large area flat panel systems.

In this tutorial, we will address the design approaches employed for operationally stable pixel circuits for flat panel imagers and organic light emitting diode (OLED) displays. It will discuss the development of oxide TFTs for displays, including interactivity and present a contrasting study with LTPS backplanes from the standpoint of system design and compensation techniques for V_T instability and OLED degradation. Besides pixel circuits and display systems, TFT-based analog and digital circuitry for signal processing and wireless power transmission are required for realization of heterogeneously integrated systems that can be realized using a combination of oxide and other technological routes on disposable/recyclable substrates. Such systems place great demand for expedient CAD tools to accurately and to reliably predict system behaviour. We review physically based CAD models, taking into account the relative dominance of the carrier transport mechanisms in the TFT, along with circuit examples.

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Printed organic TFT sensor tags

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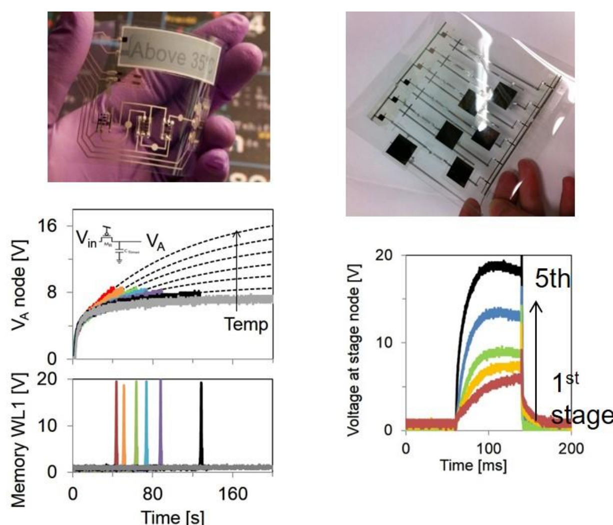
***Abstract*—Integrated OTFT circuits for sensor tags were implemented by all-additive solution processes. We took processing steps that improve the reliability of the fabrication process. The effect of device variations on the yield was evaluated, to account for the constraints of existing OTFT processes.**

Keywords—inkjet printing, organic thin film transistors

Digital, additive printing of electronic materials allows rapid, highly customizable fabrication, and low-cost printed electronics are compelling for internet-of-things applications that require large volume of distributed devices, such as in sensor networks and smart packaging. With the recent improvements in solution electronic inks, it is now possible to build independent sensor systems out of printed thin-film devices. In this tutorial I will discuss the design rules we learned in the course of developing the fully printed sensor platform.

One of the prototypes (Fig. 1) is a temperature sensor tag [1] consisted of a printed thermistor bridge, a threshold control circuit, and non-volatile memories. The threshold control circuit is based on inkjet printed complementary transistors, and the non-volatile memories are capacitors with ferroelectric polymer dielectric. When the thermistor temperature exceeds a pre-set threshold (above 35°C or below 8°C), the control circuit is triggered to generate a pulse to write into the memory. This temperature sensor tag is self-contained and will be applicable to packaging or environmental monitoring applications.

Fig. 1. OTFT temperature sensor tag (left). Pulsed voltage multiplier (right).



In electronic systems, components often require different supply voltage for operation. In order to meet this requirement and to optimize power consumption for flexible electronics, a pulsed voltage multiplier [2] is implemented to boost the voltage at specific circuit nodes above the supply voltage. A five-stage pulsed voltage multiplier is shown to provide an output voltage up to 18 V from a supply voltage of 10 V, with minimum 10 ms pulse rise time for a 70 pF load. The printed multiplier allows a single power source to deliver multiple voltage levels and enables integration of lower voltage logic with components that require higher operating voltage, for example, in the case of recording data into memory cells in sensor tags.

Lastly, a readout circuit based on a single-OTFT gain stage is demonstrated for reading ferroelectric (FE) nonvolatile rewritable memories. It was observed that high gain is not required for the readout circuit, due to the large difference in polarization charge between FE memory states. The circuit uses few OTFTs, which leads to higher yield, and does not require matching.

In addition to demonstrating the circuit performance, I will discuss some approaches to tackle the challenges of device variations and stability in printed devices [3], to improve the reliability of the fabrication processes and accelerate the development of printed electronics.

ACKNOWLEDGMENT

The author is grateful to her colleagues D. Schwartz, P. Mei, S. Ready, G. Whiting, J. Veres, and R. A Street at Palo Alto Research Center and Thin Film Electronics for funding the sensor tag development.

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Biosensors Based on Thin Film Transistors

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Abstract— **Thin film transistors have shown promising applications as sensors due to their high sensitivity, small size and the feasibility for multiplexing, in which solution-gated transistors are excellent potentiometric transducers for biosensors. Solution-gated transistors normal have no gate dielectric and the gate voltages are applied directly on the solid/electrolyte interfaces or electric double layers near the channel and the gate, which lead to very low working voltages (about 1 V) of the transistors. On the other hand, the devices can be easily prepared by solution process or other convenient methods because of the much simpler device structure compared with that of a conventional field effect transistor with several layers. Many biosensors can be developed based on the detection of potential changes across solid/electrolyte interfaces induced by electrochemical reactions or interactions. The devices normally show high sensitivity due to the inherent amplification function of the transistors. In this talk, I will introduce several types of biosensors studied by our group recently, including DNA, glucose, dopamine, uric acid, cell, and bacteria sensors, based on solution-gated organic electrochemical transistors and graphene transistors. The biosensors show high sensitivity and selectivity when the devices are modified with functional nano-materials (e.g. graphene, Pt nanoparticles) and biomaterials (e.g. enzyme, antibody, DNA) on the gate electrodes or the channel. Furthermore, the devices are miniaturized successfully for the applications as sensing arrays. It is expected that the solution-gated organic transistors will find more important applications in the future.**

Keywords—thin film transistor; biosensor; organic semiconductor; graphene

ACKNOWLEDGMENT

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Electron Devices Society: Mission and Technical Activities

Samar K. Saha

President, IEEE Electron Devices Society

Abstract–The IEEE Electron Devices Society (EDS) is a volunteer-led and volunteer-driven dynamic Society. The mission of EDS is to promote excellence in the field of electron devices for the benefit of humanity. For over 60 years this mission has been achieved through volunteer involvement and dedication. At EDS, we realize our mission in many ways: conferences, publishing, education, and technical recognition. The EDS activities include all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications. Also, EDS provides its members with critical resources, community-building opportunities, and support not available through any other organization or society.

The EDS has been a proud cosponsor of the CADTFT conference since its inception in 2008 at Cambridge, UK where it has been held as a workshop on *Compact Thin-Film Transistor Modeling for Circuit Simulation*. This workshop has transformed into CADTFT conference to offer display communities a forum to present and discuss all aspects of TFT Technology, modeling, and design. Attend this session to learn how EDS is evolving to meet the changing needs of the electron devices technical community, to discover how members can get more involved in the life and work of the Society, and to share your thoughts, insights, and feedback with EDS's volunteer leaders and staff. In this talk, the EDS technical activities and opportunities offered to its general membership will be discussed.

Design Tools for TFT Circuits and Systems*

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***Abstract*— This talk will review major developments in thin film transistor modeling for computer-aided design of circuits and systems. Based on the progress made in recent years, we have successfully developed a Verilog-AMS model called the CAMCAS model, which supports the computer-aided-design and simulation of oxide-TFTs, with the potential to be extended into other types of TFT technology families.**

Keywords—compact models, oxide TFTs, SPICE, Verilog

I. Introduction

The growing maturity of thin film transistor (TFT) technology coupled with newly emerging materials and processes are enabling integration of circuits and systems for a new generation of applications. The design of systems places great demand for fast simulation tools to accurately and reliably predict system behavior.

Significant effort has been invested in modeling of TFTs for various semiconductor technologies, starting with amorphous silicon, and then to polysilicon, organics and recently metal oxides (see [1] and references therein). In particular, several TFTs SPICE models have been developed. Specifically the model developed by Rensselaer Polytechnic Institute, also known as the RPI model, has become a commercial standard supported by many simulation platforms including SmartSpice, HSPICE, Spectre, etc. However, no CAD tool for organic and metal-oxide TFTs has yet to become a standard. This is due to the performance improvements in materials and device structures, which makes model synthesis a dynamic process.

II. Physically-Based Modeling approach

Our efforts have primarily evolved around physically-based approaches so that the models developed are simple and accurate with a minimum number of fitting parameters. The most well-studied material for TFTs is amorphous silicon. Here several models have been developed based on different distributions of deep states and tail states of the semiconductor to describe static and dynamic behavior for the above and sub-threshold regimes, including other properties such as trap related V_T-shift and the off current. Without doubt, the RPI model captures most of the device properties leading to satisfactory simulation results, and thus has been widely used.

Models for organic transistors are based on multiple trapping and release (also referred to as trap-limited conduction) as well as variable range hopping. However, the underlying physics used in the model can differ due to the diverse use of materials in the TFT, ranging from gate insulation and semiconductor layer to source/drain metallization and passivation. Therefore a trend has emerged in which the efforts are to develop a unified but less physical model.

As for metal oxide TFTs, modeling efforts are still in their infancy, although there is growing interests in the area for implementation of circuits and systems. In what follows, early efforts in compact models for CAD of oxide TFTs are reviewed.

III. The Cambridge TFT Model

Compared with amorphous silicon TFTs, the properties of the oxide materials system are unique and have to be captured. For example, localized traps or band tail states in oxides do not exist to the same extent as amorphous silicon. Their tail state density is much lower and hence trap-limited conduction is generally not as significant as in the amorphous silicon TFT. In addition, more complex systems such as amorphous indium gallium zinc oxide (a-IGZO) can have compositional disorder due to random distribution of metal constituents. This gives rise to potential barriers above the conduction band minima leading to percolation conduction [14], [16], [24].

In the presentation, we will present compact models for the terminal current-voltage behavior taking into account the different transport mechanisms in the device for the above- and sub-threshold regimes of TFT operation. The former is based on a mobility model that combines trap-limited conduction with percolation conduction. The sub-threshold regime takes into account diffusion and drift current components. Based on this, a unified model will be presented that covers both regimes described by a single expression that uses a reference voltage V_{FB} rather than V_T. Good agreement with measured terminal characteristics is obtained over the entire range of $V_{GS} > V_{FB}$ for the test TFTs with an a-IGZO channel. We will compare the differences between Verilog-AMS and SPICE from the standpoint of compact device modeling, and present the implementation of the Cambridge TFT compact model for oxide TFTs in Verilog-AMS for Spectre simulation.

Reference

Xiang Cheng, Sungsik Lee, Guangyu Yao, Arokia Nathan, "TFT Compact Modeling," IEEE/OSA JDT, vol. 12, No. 9, pp. 898-906, 2016.

*This abstract is a summary of the work published recently – see Reference [1] – and will form the basis of the plenary lecture.

Heterogeneous Integration of X-tronics: Design, Automation and Education

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Abstract

Advances in photonics, flexible electronics, emerging memories, etc. and Si electronics' integration with these devices have enabled new classes of integrated circuits and systems with enhanced functionality, greater performance, smaller footprint, or lower power consumption. Driving greater integration of such heterogeneous X-tronics can facilitate the continued proliferation of low-cost micro-/nano-systems for a wide range of applications. However, achieving their large-scale integration will require design ecosystem and design automation tools/methodologies much like those that enabled electronic integration in previous decades.

In this talk, I will briefly introduce two recent Manufacturing Innovation Institutes, on Integrated Photonics and on Flexible Hybrid Electronics respectively, and a research center on developing 3D Hybrid CMOS-memristor circuits, which bring together academia, industry, and federal partners to increase manufacturing competitiveness in these areas. I will then focus on their design and design automation efforts and highlight the needs, challenges and opportunities of developing a robust design ecosystem for X-tronics integration. I will also share the educational challenges of talent development for X-tronics design and automation.

Biography

K.-T. Tim Cheng received his Ph.D. in EECS from the University of California, Berkeley in 1988. He has been serving as Dean of Engineering and Chair Professor of ECE and CSE at Hong Kong University of Science and Technology (HKUST) since May 2016. He worked at Bell Laboratories from 1988 to 1993 and joined the faculty at Univ. of California, Santa Barbara in 1993 where he was the founding director of UCSB's Computer Engineering Program (1999-2002), Chair of the ECE Department (2005-2008) and Associate Vice Chancellor for Research (2013-2016). His current research interests include design automation for photonics IC and flexible hybrid circuits, memristive memories, mobile embedded systems, and mobile computer vision. He has published more than 400 technical papers, co-authored five books, adviced 40+ PhD theses, and holds 12 U.S. Patents in these areas. He served as Director for US Department of Defense MURI Center for 3D hybrid circuits which aims at integrating CMOS with high-density memristors.

Cheng, an IEEE fellow, received 10+ Best Paper Awards from various IEEE and ACM conferences and journals. He has also received UCSB College of Engineering Outstanding Teaching Faculty Award. He served as Editor-in-Chief of IEEE Design and Test of Computers and was a board member of IEEE Council of Electronic Design Automation's Board of Governors and IEEE Computer Society's Publication Board.

PI04

Recent progress in TFT compact modeling and parameter extraction techniques

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PI05

High Performance Organic Field-Effect Transistors and Circuits

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PI06

Compact Modeling of Organic/Polymeric Thin Film Transistors - Past, Present and Future

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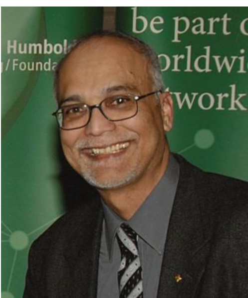
In the past few decades, the field of flexible organic/polymeric electronics has advanced significantly. This has been primarily because of improvements in the quality organic/polymeric materials after processing, as well as the processing techniques and technologies. For example, roll-to-roll, sheet-to-sheet or printing technologies are being proposed as suitable manufacturing candidates because they can be carried out at room temperature, do not require the kind of clean room environment needed for traditional semiconductor manufacturing, and are very suitable for very low-cost, high volume production. Further, these advances are mostly stimulated by the promise of lighter and more robust devices and systems for applications that include large-area electronics, active matrix large-area displays, large-area solar cells, interactive displays, and conformable sensors and actuators. However, despite these advances, there remain challenges in the large-scale transfer of research prototypes into manufactured products. One of manor the limitations is the lack of accurate compact models for organic/polymeric thin film transistors with associated parameter extraction techniques. In this presentation, we will discuss some of the recent compact models and illustrate the merits and limitations of several of them. We will discuss in detail our progress in developing industry-viable static and dynamic compact models for flexible transistors with predictable performance. Finally, we will present several modeling challenges including hysteresis and contacts effects, as well as models that can predict stability, reliability, and lifetime.



Dr. M. Jamal Deen is Distinguished University Professor, Senior Canada Research Chair in Information Technology, and Director of the Micro- and Nano-Systems Laboratory, McMaster University. His current research interests are nanoelectronics, optoelectronics, nanotechnology and their emerging applications to health and environmental sciences. Dr. Deen's research record includes more than 520 peer-reviewed articles (about 20% are invited), two textbooks on "*Silicon Photonics- Fundamentals and Devices*" and "*Fiber Optic Communications: Fundamentals and Applications*", 6 awarded patents that have been used in industry, and 16 best paper/poster/presentation awards. Over his career, he has won more than fifty awards and honors.

As an undergraduate student at the University of Guyana, Dr. Deen was the top ranked mathematics and physics student and the second ranked student at the university, winning the Chancellor's gold medal and the Irving Adler prize. As a graduate student, he was a Fulbright-Laspau Scholar and an American Vacuum Society Scholar. He is a Distinguished Lecturer of the IEEE Electron Device Society for more than a decade. His awards and honors include the Callinan Award as well as the Electronics and Photonics Award from the Electrochemical Society; the Distinguished Researcher Award from the Province of Ontario; a Humboldt Research Award from the Alexander von Humboldt Foundation; the Eadie Medal from the Royal Society of Canada; McNaughton Gold Medal (**highest award for engineers**), the Fessenden Medal and the Ham Education Medal, all from IEEE Canada IEEE Canada In addition, he was awarded the three honorary doctorate degrees in recognition of his exceptional research and scholarly accomplishments, professionalism and service. Dr. Deen has also been elected Fellow status in ten national academies and professional societies including The Royal Society of Canada - The Academies of Arts, Humanities and Sciences (**the highest honor for academics, scholars and artists in Canada**), IEEE, APS (American Physical Society) and ECS (Electrochemical Society). Currently, he is serving as the elected President of the Academy of Science, The Royal Society of Canada.

INV1-1

TFT Recent Progress and Its Applications

Yanzhao Li

BOE, China

Progress on Flexible & Printed OLED Displays and their TFT Backplane Technology

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***Abstract*—We report a high performance oxide TFT with a Lanthanide rare earth doped In-Zn-O (Ln-IZO) semiconductor material as the active layer. The Ln-IZO TFT with BCE structure exhibit a high field-effect mobility of 40 cm^2 V^{-1} s^{-1}. Then, we developed a 2-inch full color flexible ink-jet printed AMOLED display driven by the Ln-IZO-TFT backplane.**

Keywords*—*oxide TFT; back channel etching; flexible display; ink-jet printing

I. Introduction

Oxide semiconductor TFTs have extensively been studied due to their merits such as good uniformity and low cost [1-2]. However, the display technology needs to be satisfied with the requirement of low power, high resolution and high frame rate, which claims the TFTs should possess higher mobility and excellent stability. In this study, we have successfully fabricated Ln-IZO TFT with high mobility and good stability using back-channel-etch (BCE) process, which could successfully drive the flexible AMOLED display.

II. Ln-IZO TFT Backplane and the Diplay

A. Device Structure

The schematic cross section of the BCE Ln-IZO TFT is shown in Fig. 1. A stacked structure of C(10 nm)/Mo(200nm) was sequentially formed by sputtering. Then, H_3PO_4-based etchant was employed to pattern the Mo film, and at the same time Ln-IZO film was protected by C. Then, O_2 plasma was used to pattern C film.

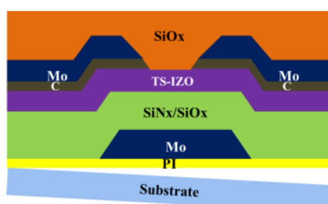

Figure 1. Schematic cross-section of the Ln-TFT with C nano-film protected BCE Structure.

B. Ln-IZO TFT performance

Fig. 2(a) show the TFT exhibits mobility (μsat) of ~40 cm^2 V/s, a Vth of 0.78 V, a SS of 0.15V/dec, and an I_{on}/I_{off} of ~10^9. The on-current of the TFTs are above 10^{-5} A and the off-current is below 10^{-13} A, which demonstrates the promise for the TFTs in the application of high resolution displays requiring a large on-current to drive pixels and a small off-current to minimize the power consumption. Fig. 2(b) and 2(c) show positive bias stress and negative bias stress stability of the Ln-IZO TFT, respectively. The results show Vth shifts of 0.92 V and less than -0.1 V under PBS and NBS for 7200 s, respectively. Finally, the flexible OLED display was fabricated shown in Fig.2.

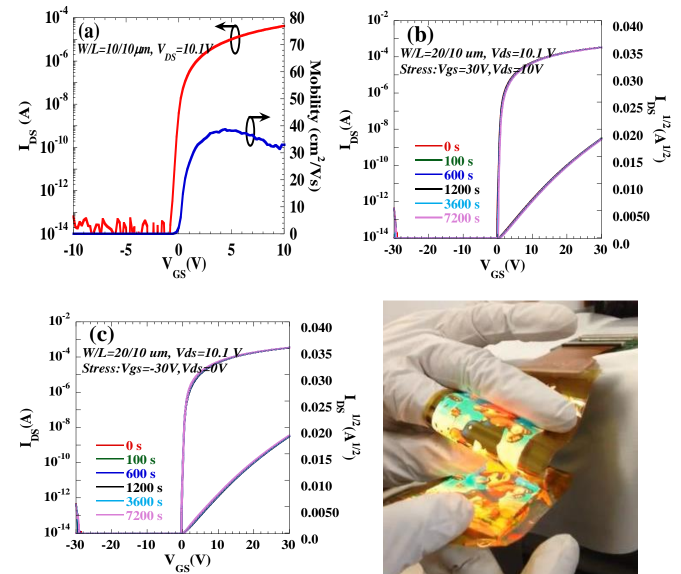

Figure 2. Ln-TFT performance and flexible AMOLED.

III. Summary

High performance BCE Ln-IZO TFT was successfully used to drive flexible AMOLED display. The BCE structure for TFT and the ink-jet printing technology for OLED can reduce the costs of AMOLEDs significantly.

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Rational hydrogenation for enhanced mobility and high reliability on ZnO-based thin film transistors: from simulation to experiment

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Abstract:

Hydrogenation is one of the effective methods for improving the performance of ZnO thin film transistors (TFTs), which originate from the fact that hydrogen (H) acts as a defect passivator and a shallow n-type dopant in ZnO materials. However, passivation accompanied by an excessive H doping of the channel region of a ZnO TFT is undesirable because high carrier density leads to negative threshold voltages.

Firstly, we report that Mg/H codoping could overcome the trade-off between performance and reliability in the ZnO TFTs. The theoretical calculation suggests that the incorporation of Mg in hydrogenated ZnO decrease the formation energy of interstitial H and increase formation energy of O-vacancy (V_O). The experimental results demonstrate that the existence of the diluted Mg in hydrogenated ZnO TFTs could be sufficient to boost up mobility from 10 to 32.2 cm^2/Vs at a low carrier density ($\sim 2.0\times10^{18}$ cm^{-3}), which can be attributed to the decreased electron effective mass by surface band bending. The all results verified that the Mg/H codoping can significantly passivate the V_O to improve device reliability and enhance mobility.

Secondly, our study examined the electrical performance of bilayer channel ZnO:H/ZnO and InGaZnO:H/InGaZnO thin-film transistors. The field-effect mobility and bias stress stability of the devices were improved by inserting of the hydrogenated ZnO or InGaZnO ultrathin layer compared to the pure oxide single channel layer device. As a consequence, a high field-effect mobility of 55.3cm^2/V s, a high on/off current ratio of 10^8, a threshold voltage of 0.7 V and a small sub-threshold swing of 0.18 V/decade has been achieved. The X-ray photoelectron spectroscopy and low-frequency noise analysis suggest that these desirable properties should be attributed to the ultrathin hydrogenation layer, which could provide suitable carrier concentration and reduce the average trap density near the channel and insulator layer interface. Meanwhile, the channel conductance of the bilayer device is controlled by thick oxide layer through formation barrier energy for electron transport at the interface of oxide:H and pure oxide layer. These improved electrical properties have represented a great step towards the achievement of transparent, high performances, and low-cost metal oxide TFTs.

Development of high performance printed ambipolar polymer complementary integrated circuits

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***Abstract*— We present way to realize high performance polymer transistors and complementary integrated circuits by developing of novel conjugated polymers, of simple bar-coating process for thin film deposition, controlling of charge injection property, and applying benign polymer dielectric layer.**

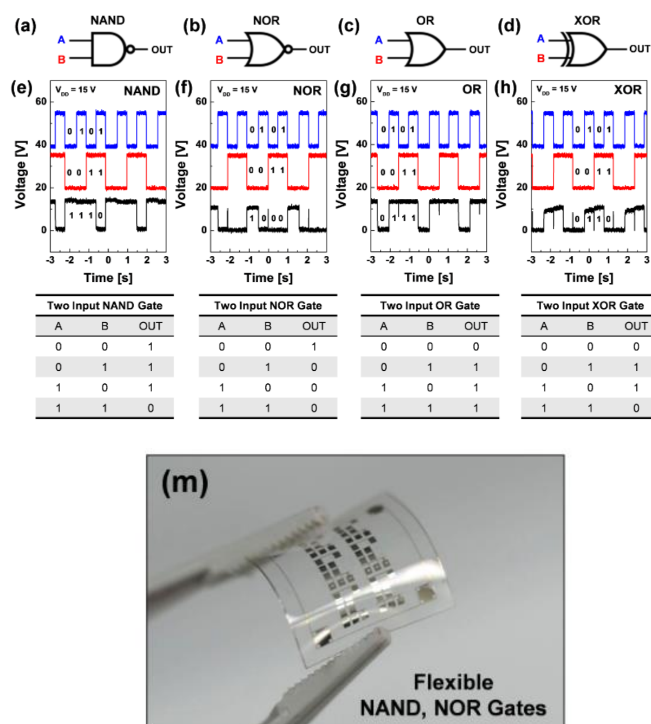
Keywords—organic field effect transistors, conjugated polymers, printed electronics

I. Introduction

Ambipolar π-conjugated polymers may provide inexpensive large-area manufacturing of complementary integrated circuits (CICs) without requiring micro-patterning of the individual p- and n-channel semiconductors. However, current-generation ambipolar semiconductor-based CICs suffer from higher static power consumption, low operation frequencies, and degraded noise margins compared to complementary logic based on unipolar p- and n-channel organic field-effect transistors (OFETs). Here we demonstrate a simple methodology to control charge injection in ambipolar OFETs via engineering of the electrical contacts. By controlling the electrode surface chemistry, excellent p-channel (hole mobility ~ 5 cm^2/Vs) and n-channel (electron mobility ~ 5 cm^2/Vs) OFET characteristics with various state-of-art conjugated polymers are demonstrated.

II. Result and Discussion

We have reported high performance printed OFETs by development of novel printing process, newly synthesized conjugated polymers, high capacitance polymer dielectrics and selective charge injection engineering techniques. High-performance, truly complementary inverters (gain > 50) and ring oscillators (oscillation frequency 10 ~ 50 KHz) based on a solution-processed ambipolar polymer are demonstrated [1]. In addition, various logic circuits such as NAND, NOR, and XOR etc. were demonstrated by optimizing gate dielectrics, printing processes, and contact resistance optimization (Fig. 1). We also introduce high performance RFID circuits, chemical sensors, and various analog and digital complementary circuits by using printed OFETs with those conjugated polymers [2-8].



Two Input NAND Gate		
A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Two Input NOR Gate		
A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Two Input OR Gate		
A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

Two Input XOR Gate		
A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Fig. 1. (a–d) Electronic circuit symbols, and (e–h) output (OUT, black solid line) versus two inputs (A and B, blue and red solid lines) voltage characteristics of the various printed logic gates;

Acknowledgment *(Heading 5)*

The preferred spelling of the word "acknowledgment" in America is without an "e" after the "g."

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The template will number citations consecutively within brackets [1]. Use the following style for references:

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Oxide-based Electric-Double-Layer Thin-Film Transistors for Neuromorphic Systems

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***Abstract*—Our brain can perform a simple cognitive task by consuming only ~20 W of power because it processes information using energy efficient, highly parallel, event-driven architectures as opposed to clocked serial processing. The fundamental building block of every nervous system is the single neuron. Neurons have intricate dendritic morphologies and receive thousands of excitatory and inhibitory synaptic inputs arriving at different dendritic locations. Realization of physical devices with synaptic/neuronal functions is of great importance for hardware implementation of neuromorphic computation system. Here, we provide a proof-of-principle artificial neuron with multiple presynaptic inputs based on a field-configurable oxide-based electric-double-layer thin-film transistor. Temporal summation (paired-pulse facilitation and high-pass filtering) is realized due to the dynamic process of the proton modulation. Regulation of dendritic summation was successfully mimicked by changing the voltage applied on the modulatory terminal. Additionally, neuronal gain control (neuronal arithmetic) in the scheme of temporal-correlated coding is also realized. Our results provide a new-concept approach for brain-inspired neuromorphic systems.**

Keywords—Oxide-based Thin-film Transistors; Synaptic devices; Neuromorphic systems

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Beyond Display: Emerging Applications of Thin-Film Transistors

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***Abstract*—This paper addresses emerging applications of thin –film transistors in X-ray imaging, tactile sensing, energy harvesting, heart rate monitoring, biometrics, and biosensors.**

***Keywords*—dual-gate thin-film transistor; X-ray imaging; tactile sensor; energy harvesting; heart rate monitoring, fingerprint sensor; biosensor**

As a fundamental building block of large-area electronics, thin-film transistor (TFT) and its relatives have enjoyed an exciting time of being explored and developed during the past three decades. As its dominant application, flat-panel display has become a multi-billion-dollar industry that keeps growing. However, the potential of TFT technology in other fields such as sensors and energy harvesting has been barely investigated and yet researched, we hereby propose to extend TFT technology to some emerging applications and summarize the recent work in low-dose digital X-ray imaging [1], highly-secure fingerprint sensing [2], tactile sensors for electronic skins [3], energy-harvesting arrays for wearable electronics [4], impulse sensor for heart-rate monitoring [5], and biosensors for Amniotic Fluid Embolism [6]. By redesigning and optimizing device structures, we aim to tackle challenges in achieving high signal-to-noise ratio, wide dynamic range and low cost the aforementioned applications generally require. A short review on these topics will be given in this talk. We will also try to elucidate device physics, establish physical and circuit models, and clarify device structure-performance relations as well as to resolve key issues in fabrication and integration.

From our study, we anticipate that the TFT technology will potentially go far beyond flat-panel display in the next one to two decades and will make significant promises in refreshing large-area electronics and fostering emerging applications in various fields (Fig. 1).

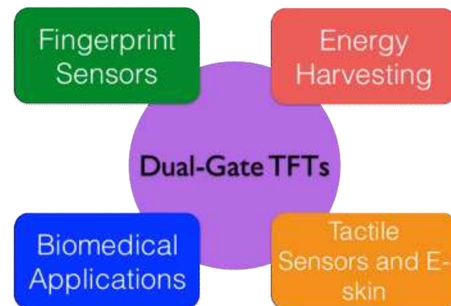

Fig. 1 Research Focus on Emerging Applications of Dual-Gate TFTs.

Acknowledgment

The graduate students in my group are acknowledged for this work including Hai Ou, Man Xu, Xinghui Liu, Emad Iranmanesh, Ahmed Rasheed, Yiwen Chen, Hantao He, and Huimin Li. I am also grateful to my collaborators: Prof. Jun Chen, Prof. Shaozhi Deng, Prof. Ningsheng Xu from Guangdong Province Key Lab of Display Materials and Technology at Sun Yat-sen Univeristy and Prof. Jeff A. Weldon from Carnegie Mellon University in US.

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Enhancing the speed of printed and direct-written polymer transistors

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***Abstract*— Organic field-effect transistors (OFET) show limited speed of operation, thus limiting their adoption in many high-frequency applications. Attempts to improve the speed of OFETs typically rely on sophisticated lithographic techniques. Here we present the combination of large-area printing processes and laser based direct-writing techniques to achieve MHz operation in polymer FETs in a completely mask-less approach.**

Keywords—organic transistor; high-frequency organic transistors; transition frequency; ac transistor operation

I. Introduction

Printed organic field-effect transitors (OFETs) have been considered for many novel applications towards large area and flexible electronics [1], since they can enable pervasive integration of electronic functionalities in all sorts of appliances, their portability and wearability. Applications are countless: from personal devices (e.g. wearable health monitoring devices) to large-area sensors (e.g. electronic skin, bio-medical devices), and smart tagging of products with radio-frequency identification tags. It is no doubt that a huge driving force comes from flexible and/or rollable displays deployable on demand, to be integrated with portable and wearable devices. However, printed OFETs fabricated with scalable tools fail to achieve the minimum speed required for example to drive high-resolution displays or to read the signal from a real-time imager, where a transition frequency (f_T), i.e. the highest device operative frequency, above 10 MHz is required. In this contribution we present effective strategies to increase f_T in polymer devices by combining only printing and laser-based direct-writing techniques. [2][3][4]

II. Large-area Coating of Nanostructured and Aligned Polymer Films

A key to enable widespread organic electronics technologies is the possibility of using high-throughput, large-area printing processes to pattern polymer semiconductors with uniform and optimized morphologies. By controlling the self-assembling properties of conjugated copolymers, in combination with simple, roll-to-roll compatible coatings, it is possible to achieve well-ordered and efficient charge-transport nanostructures over large-areas [2]. In particular, by exploiting the one-dimensional self-assembly of model conjugated polymers, such as naphthalene diimide based co-polymers, highly controlled printed anisotropic thin films with excellent transport properties are demonstrated. By controlling the ink flow directionality with a bar-coating deposition technique, shear-aligned thin films with a highly oriented functional surface are realized at a coating speed of few meters per minute, without the need for additional post-processing steps. This approach produces a marked FET mobility anisotropy and greater performance uniformity with respect to the spin-coating deposition, and excellent electron mobility along the printing direction, with a remarkable maximum value of 6.4 $cm^2V^{-1}s^{-1}$ and an average value of 4.1 $cm^2V^{-1}s^{-1}$. The simple adoption of this fast coating approach allows to strongly enhance the highest operational frequency of FET devices, achieving a transition frequency of 3.3MHz.

III. Direct-Written Polymer Transistors

By combining printing and laser-based direct-writing techniques, additional strategies to boost the transition frequency of polymer based devices can be pursued. First, by combining inkjet printing and femtosecond laser ablation [3] to obtain small channel lengths, all-polymer FETs operating in the MHz regime can be fabricated on plastic without the use of any mask. In particular, an engineered layout of the contacts allows to achieve a transition frequency of 5 MHz. [4] Alternatively, narrow, micron-scale metallic electrodes can be sintered on plastic through femtosecond laser sintering. The combination of such electrodes with fast-coated polymers allow to achieve the higher transition frequency for a mask-less fabricated polymer transistor to date, reaching 20 MHz.[5]

Acknowledgment

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Printed short-channel thin-film transistors

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***Abstract*—In this report, metal oxide thin-film transistors (TFTs) with channel lengths of 3.5 ± 0.7 μm were successfully fabricated with a common inkjet printer without any photolithography steps. Hydrophobic CYTOP coffee stripes, made by inkjet-printing and plasma-treating processes, were utilized to define the channel area of TFTs with channel lengths as short as ~3.5 μm by dewetting the inks of the source/drain (S/D) precursors. The inkjet-printed shortchannel TFTs exhibited a maximum mobility of 4.9 cm^2 V^{-1} s^{-1} and an on/off ratio of larger than 10^9.**

Keywords—inkjet printing; short-channel; thin-film transistors

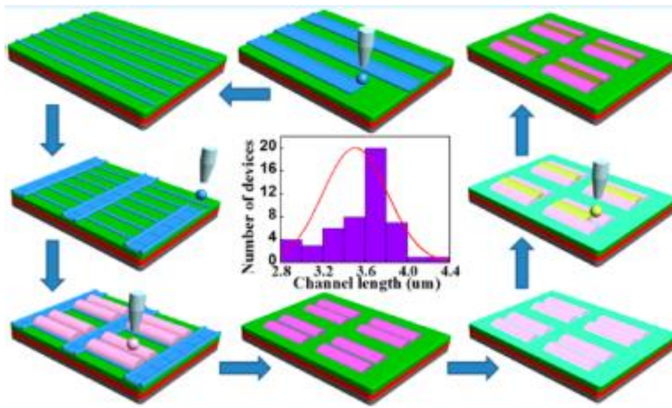

Fig. 1. Flow-process diagram of the coffee-ring defined method for inkjet-printed metal oxide TFTs.

Short-channel electronic devices several micrometers in length are difficult to implement by direct inkjet printing due to the limitation of position accuracy of the common inkjet printer system and the spread of functional ink on substrates. Herein,,short-channel InOx TFT arrays with channel lengths

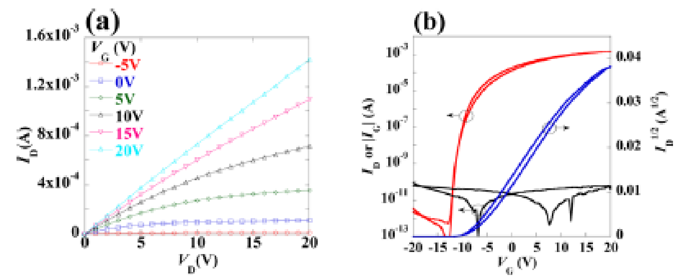

Fig. 2. (a) Typical output and (b) transfer characteristics of the printed short-channel TFT.

of 3.5 ± 0.7 μm were fabricated using the inkjet printing method. Different from the short-channel fabricating approaches reported elsewhere, ultrafine hydrophobic CYTOP coffee stripes, obtained by inkjet-printing and plasma-treating processes without any photolithography steps, were used to define the channel length of the TFTs. Additionally, PVA was first introduced to modify the surface of ITO and AlOx:Nd to regulate the wetting property and control the spread of droplets of the InOx ink. This work provides a route toward fabricating short-channel MO TFTs in a costeffective manner.

ACKNOWLEDGMENT

The authors are grateful to the National “863” Project of China (Grant no. 2014AA033002), the National “973” Project of China (Grant no. 2015CB655000).

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TCAD for compact model development? Get real!

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***Abstract*—An argument for the use of physics based continuous Technology Computer Aided Design (TCAD) models for the development of advanced TFT compact models will be advanced. The significant opportunities TCAD software gives to compact model developers will be presented. A number of scenarios to illustrate the scope of integrated TCAD to SPICE flow in the development of new compact models will be reviewed.**

Keywords—TCAD, Compact Models, TFT.

I. Introduction

Standard oxide and organic thin film transistor TFT compact models are needed to advance the large area electronic design sector. The availability of such models within process design kits (PDK), will enable many designers to enter this space. Designer scan specify new materials for their products and applications. This will in turn increase adoption and innovation in this technology.

II. Why TCAD

In order to create physics based SPICE models that can predict the behavior of the new TFT materials and devices, intimate knowledge of the charge transport is required under a variety of conditions. TCAD offers three key advantages:

- Users can bring to bear extensive semiconductor device physics and material related models and parameters. These have been developed through many years of accumulated knowledge and calibrated control experiments.
- Users gain unique insight into the charge transport in TFT devices under various bias conditions, both dc and transient. Parasitic elements are implicit in these models. Although complimentary to lab based measurements, such insight remains over and beyond what can be measured in the lab.
- Extensive exploration of the available design space can be performed and automated. These cover material issues, device architecture design issues, and beyond into circuit and product design. Optimum parameter compromises can be "discovered' via complex design of experiment (DOE) and optimization strategies.

The application of TCAD to the development of UOTFT compact model [1-6] from Silvaco will be illustrated. A number of example scenarios that reveal the link of the transfer and output characteristics, as well as the parasitic capacitance of the various contacts, to the fundamental material properties of these devices will be reviewed.

III. Software Flow

Having access to seamless software flow and tools to perform a matrix of TCAD simulations in a DOE split lot presents unique opportunities to produce physics based compact models. Key to this, is the integration of the compact model parameter extraction and fitting software Utmost IV [7-8] via the JavaScrip capability. This will quickly reveal the limits of the available features in the compact model. This will also serve to accelerate the development of extra features based on sound device semiconductor physics.

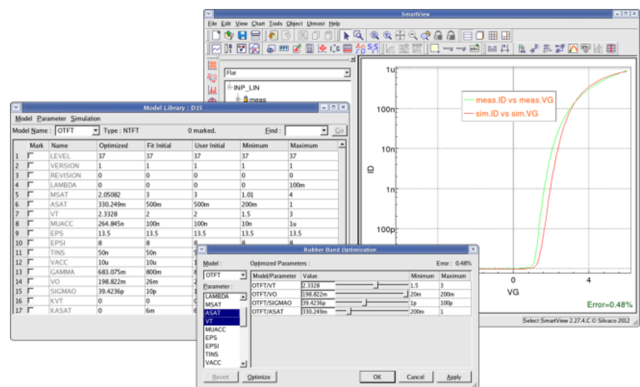

Fig. 1. Example fitting of IdVg data to the UOTFT model in order to obtain model parameters.

Acknowledgment

The authors would like to acknowledge the support of the UK Advance Manufacturing Supply Chain Initiative (AMSCI) for the SCOPE: Supply Chain Opportunity for Printable Electronics (Reference Number 33084-233301) project as well as the EU Horizon 2020 MSCA-RISE SEP-210168496 DOMINO project.

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TCAD and circuit simulation of thermal effects in source-gated transistors

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***Abstract*—Schottky contact Source-Gated Transistors have excellent characteristics for low-power, large area analog and digital circuits. The nature of the current control mechanism makes the drain current inherently temperature-dependent. This paper describes recent device- and circuit-level simulation results aimed at temperature effect optimization.**

***Keywords*—schottky contact; thin-film transistor; source-gated transistor; TCAD; logic gate; temperature effects; optimization**

I. INTRODUCTION

Source-gated transistors (SGTs) [1] use a potential barrier at the source to control the current through the device. Most frequently, this barrier is a Schottky contact. Schottky SGTs are easy to fabricate and have useful properties for both analog and digital circuits [1, 2], such as low-voltage saturation, flat saturated characteristics and superior stress stability. This philosophy can be applied to other material systems [1-3].

II. TEMPERATURE EFFECTS IN SGTS

Silvaco Atlas was used [4-5] to perform TCAD and circuit simulations on poly-Si SGTs and complementary inverters.

The presence of the reverse-biased Schottky barrier at the source leads to significant temperature dependence of drain current in these devices. Due to device electrostatics, two current injection mechanisms exist at the source. The edge of the source injects current which is highly temperature and electric field dependent. This is problematic in principle, as it may lead to a runaway self-heating process, as the highly temperature-dependent current is injected in the area of the device most sensitive to temperature, the low-conductance depletion region at the edge of the source.

Conversely, the bulk produces current of low temperature dependence and practically insensitive to drain electric field. By allowing this bulk current to dominate, devices with high intrinsic gain and low temperature dependence can be designed. Incorporating a field relief structure into the source electrode also reduces both the temperature and field dependence. Successful device optimization can reduce the positive feedback effect of self-heating to negligible effects.

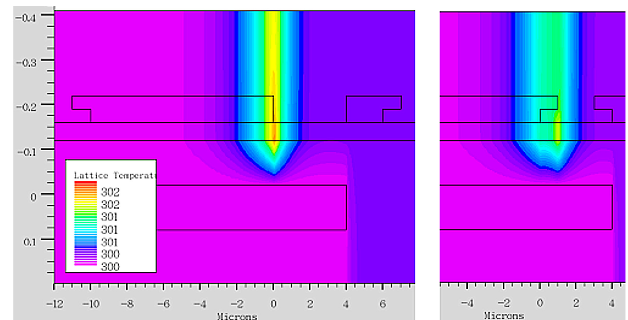

Fig. 1. Temperature hot-spots form at the edge of the source closest to the drain, and can be minimized using a field-relief structure, from [4].

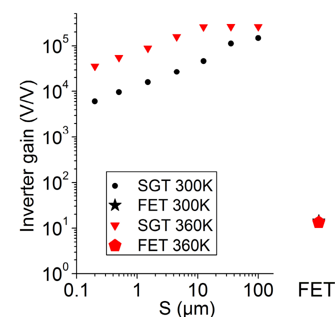

Fig. 2. Complementary inverters made with polysilicon SGTs have significantly higher gain than equivalent FET circuits. SGT drain current increases dramatically with temperature, which leads to increased transconductance. As the current is controlled by the depletion region at the source, output conductance in saturation remains low and intrinsic gain rises with temperature. From [5].

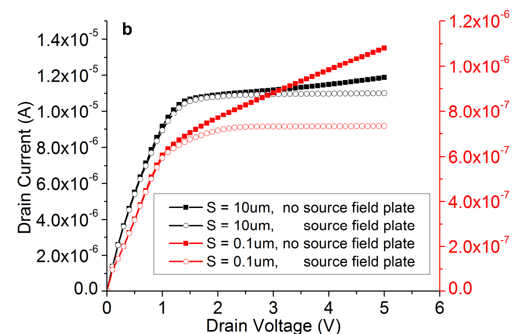

Fig. 3. Current from the bulk of the source has a lower temperature coefficient as well as lower dependence on the drain electric field, compared to current injected at the edge of the source. SGTs with longer sources, or which incorporate field plates into the source electrode have significantly lower output conductance resutling in superior intrinsic gain; from [4].

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Oxygen Adsorption Effects of Metal Oxide Thin Film Transistors

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***Abstract*—Effects of oxygen adsorption on both the device performance and stability of metal oxide thin film transistors (TFTs) are investigated. The adsorbed oxygen molecules at the back channel of the device exist as O_2^-s by capturing electrons from the channel and as O_2s if charge transfer does not take place. The O_2^-s can induce a depletion layer at the back surface, and an increase of threshold voltage (V_{th}) can be observed as a result. During positive gate bias stress (PBS), the stability measured in oxygen ambient is worsened than in vacuum which is attributed to the transition from the adsorbed O_2s to O_2^-s.**

Keywords—thin film transistors; metal oxide semiconductor; oxygen adsorption; reliability

I. INTRODUCTION

Metal oxide thin-film transistors (TFTs) have attracted great attention due to their superior performances. However, the instability is still one of the major issues [1]. In this work, effects of oxygen adsorption on both the device performance and the stability under PBS of metal oxide TFTs are studied.

II. RESULTS AND DISCUSSION

Passivation-free bottom gate staggered a-IGZO TFTs were fabricated with the a-IGZO sputter-deposited at different oxygen flow rates (R_Os). Fig. 1 shows the time-dependent threshold voltage (V_{th}) variations for devices with a-IGZO deposited at (a) low and (b) high R_O once O_2 is introduced into the vacuum chamber. As shown in Fig. 1(a), the low-R_O devices show a remarkable V_{th} increase with measurement time. It indicates that oxygen molecules can be chemically adsorbed by capturing electrons from the a-IGZO and exist in the form of O_2^-s as shown in the inset. In this way, a depletion layer is then formed at the back surface, leading to the increase of V_{th}. However, as shown in Fig. 1(b), devices with a-IGZO deposited at high R_O show no significant V_{th} change, suggesting the physically adsorbed O_2 molecules without charge transfer. The different V_{th} variations can be explained by the higher intrinsic electron concentration of the a-IGZO channel for the low-R_O devices [2]. When PBS is applied, a more significant threshold voltage shift (ΔV_{th}) is observed in oxygen ambient than in vacuum for devices with different R_Os as shown in Fig. 2. As electron concentration at the back channel increases under PBS, those physically adsorbed oxygen molecules convert to be the chemically adsorbed species, aggravating the ΔV_{th} induced by PBS.

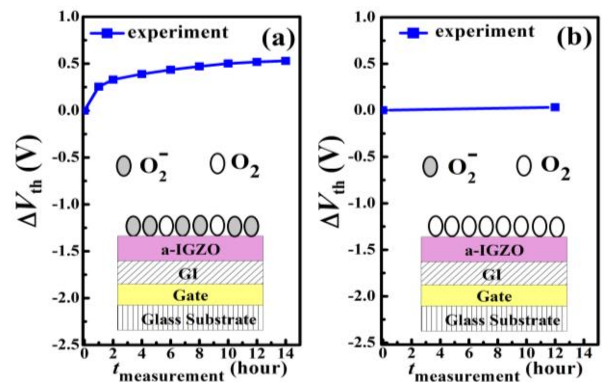

Fig. 1. V_{th} variations as a function of measurement time once O_2 is introduced into the vacuum chamber for a-IGZO TFTs with channel layer deposited at (a) low and (b) high R_O. The inset shows the corresponding schematic diagram.

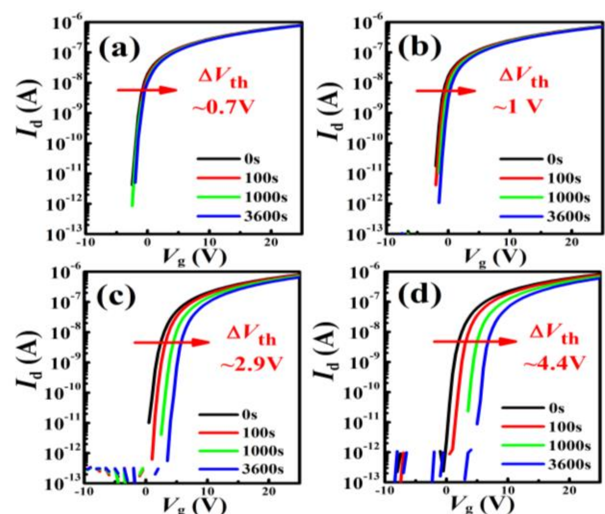

Fig. 2. Evolution of transfer characteristic curves as a function of stress time under PBS of 30V for low-R_O sputtered IGZO TFTs measured in (a) vacuum and (b) O_2 ambient, and for high-R_O devices in (c) vacuum and (d) O_2 ambient.

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Investigation on the stability of ambipolar SnO TFTs

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***Abstract*—The investigation on the stability issues of ambipolar SnO TFTs was carried out in this paper. On one hand, the TFTs showed good stability with marginal changes in the transfer characteristics under negative gate-bias stress (NGBS). On the other, however, the transfer curves under positive gate-bias stress (PGBS) condition presented parallel and positive shift with no degradation in field-effect mobility and subthreshold swing. The stress duration-dependent turn-on voltage shift induced by PGBS under different stress voltages and temperatures could be described by the stretched exponential model, in which the relaxation time and activation energy was extracted to be 1.6×10^4 s and 0.43 eV, respectively.**

Keywords—SnO; Ambipolar TFTs; Gate-bias stress; Stablity

I. Introduction

It is well established for amorphous silicon (a-Si) or a-IGZO TFTs that prolonged application of gate-bias on the TFTs can lead to the instability phenomena, known as gate-bias stress effect.[1-4] This effect manifests itself as the changes in the threshold voltage, the subthreshold slope, and the field-effect mobility. In addition, it has been proved that the stability issue can be improved through different strategies such as annealing treatment or device passivation. Likewise, for ambipolar SnO TFTs, the electrical stability issue is also of paramount importance for practical logic circuit applications. But nevertheless, there are few reports on the bias-stress stability of ambipolar SnO TFTs. In this paper, the electrical stability of ambipolar SnO TFTs under gate-bias or temperature stress was investigated.

II. Experimental

Bottom-gate TFTs using SnO films (20 nm) as the channel layers were fabricated on thermally oxidized SiO_2/n^+-Si substrates, with the SiO_2 (110 nm) and the n^+-Si as the gate insulator and gate electrode, respectively. The Ni/Au (100/50 nm) films used as drain/source electrodes were deposited by electron-beam evaporation. All the films were patterned by the shadow masks. The width-to-length ratio of the TFTs is 6, with a width of 600 μm. The fabricated devices were annealed finally at 200 °C for 1 hour in air.

III. Results and Discussion

The anisotropic carrier trapping behaviors were observed for the ambipolar SnO TFTs under gate-bias stress. The TFTs displayed good stability under NGBS, whereas the transfer curves under PGBS exhibited positive and parallel shift (see Figure 1) with no degradation in the field-effect mobility and subthreshold voltage swing. The V_{ON} shift under PGBS is considered to be originated from the charge trapping within the SnO channel layer or/and at the SnO-SiO_2 interface. The stretched exponential formula was proposed for the PGBS stability modeling, similar to the threshold voltage shift of a-IGZO and a-Si TFTs. The relaxation time and the activation energy for the SnO TFTs was extracted to be 1.6×10^4 s and 0.81 eV, respectively.

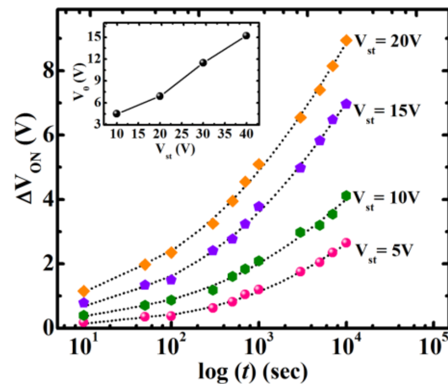

Fig. 1 Dependence of ΔV_{ON} on t at various V_{st}. The dotted line is the data fitting by the stretched exponential equation. Inset shows the dependence of extracted V_0 on V_{st}.

Acknowledgment

This work is supported by the National Natural Science Foundation of China (Grant No. 61274095).

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Process Design Kit and EDA Tools for Organic/Printed Electronics

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***Abstract*—This paper proposes a methodology to design organic/printed electronics digital circuits. The methodology is based on creating a Process Design Kit compatible with EDA tools allowing the design of digital circuits.**

Keywords—organic/printed electronics; EDA tools; Process Design Kit (PDK); digital circuits

I. INTRODUCTION

Printed/Organic technologies are maturing technologies. Most available results in terms of digital designs for organic/printed electronics is done from scratch using a full custom approach where all the devices and connections are drawn by the designer without making use of design automation tools. However, more mature technologies, like CMOS, make extensive use of design automation tools. In this paper we investigate means to adapt design automation methodology from CMOS to printed/organic technologies

II. PROPOSED METHODOLOGY

A. Creating a PDK

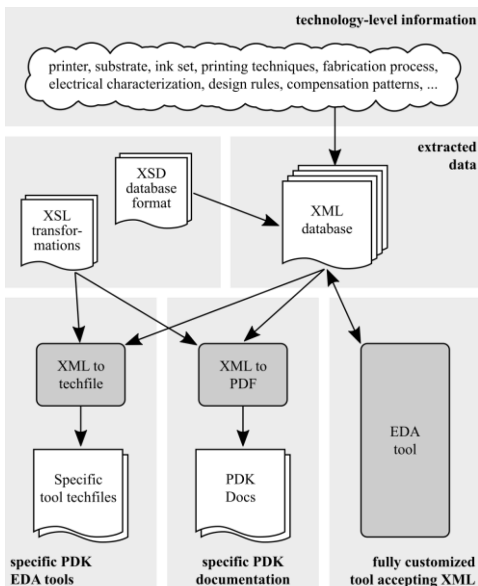

Fig. 1. Creation of a PDK from XML database

The creation of the design kit involves the design and fabrication of several test structures. Once these structures are fabricated, they are characterized and parameters are extracted. Our methodology is presented in Fig. 1, which illustrates that extracted parameters are stored in XML format, and then converted to specific files needed for EDA tools, as well as manuals of the design kits in PDF format.

B. Design with EDA tools

The use of design automation tools can be made as a traditional place and route flow as shown in Fig. 2. Notice that to enable this flow, several standard files such as .liberty, .LEF, as well as the design rules have to be provided in a format legible to commercial tools. As a proof of concept, Fig. 3 presents a layout of a digital circuit obtained with the design kit we have developed for an organic/printed technology.

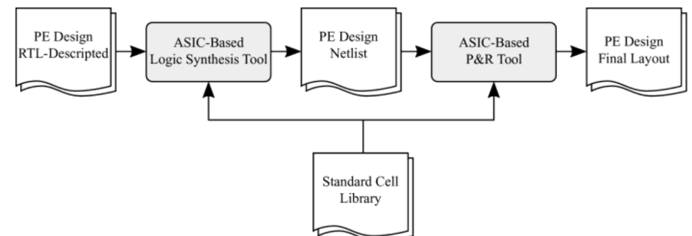

Fig. 2. Standard cell Place and route flow for standard cell.

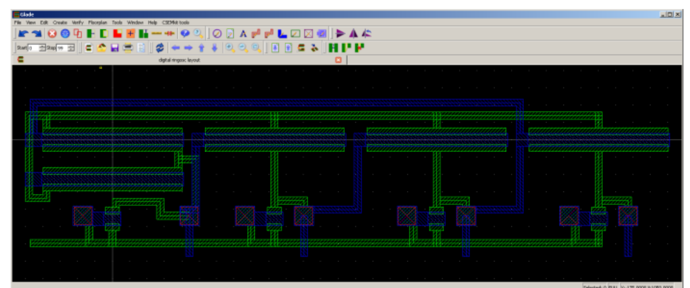

Fig. 3. Layout of a digital circuit obtained with the design kit using commercial EDA tools.

ACKNOWLEDGMENT

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Oxide-TFT Circuit Design for High-Reliability Flexible Electronics

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The flexible electronics including displays and sensors are regarded as essential to wearable appliances and also expected to create innovations of traditional consumer electronics. The reliability of the elements comprising the flexible elements under the mechanical stress as well as the electrical and thermal stresses is one of primary issues. Accordingly, a variety of studies have been performed to obtain a sufficient level of reliability, but most of the approaches have been tried from the sides of the material, process, and device structures. In this talk, we will discuss how circuit design can help achieve more reliable flexible electronics. Several leading display companies already announced prototypes of flexible displays, but all the circuitry are mounted on the separate printed circuit boards and connected to the pixel arrays [1]. Because this configuration puts a fundamental limitation on the flexibility, at least we need to integrate gate drivers, even though it is almost impractical to integrate all the circuitry on the substrate with TFTs. Previously, we proposed the concept of “carry-free” gate driver, which is robust against the mechanical stress. However, it needs much more numbers of input signals than traditional ones, thus we have made more progress to reduce the number of input signals while maintaining the advantage of the carry-free characteristic [2]. In addition, we will also discuss the transistor sizing in terms of the TFT reliability. We found that the scanning signal for active-matrix displays can allow asymmetric rising and falling times, which will give us a chance to rethink about the transistor sizing for the gate driver [3]. Another topic of this presentation is about how to construct the logic circuits. It is well known that in a traditional static circuit power consumption is drastically increased and the output signal range is reduced. We also found that the static circuit is unfavorable for the mechanical reliability.

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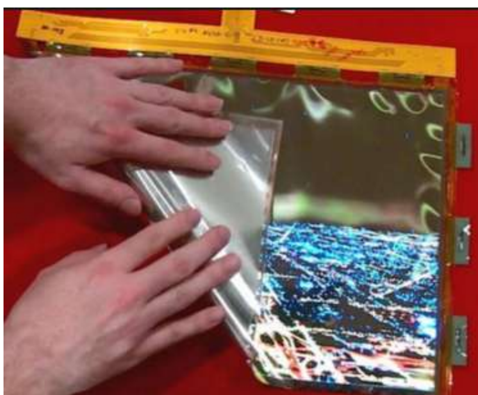

Fig. 1 A prototype of a flexible display. All the circuitries are mounted on the printed circuit boards [1].

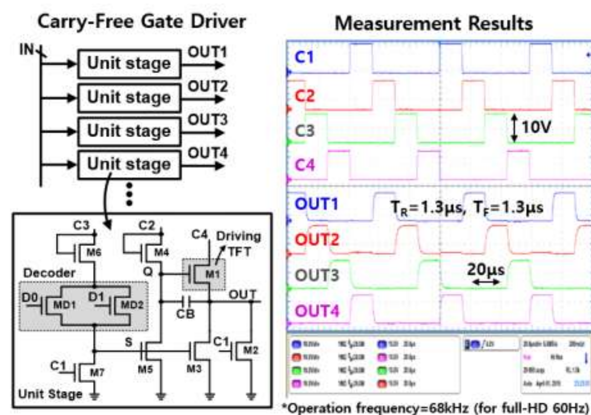

Fig. 2 Concept of the carry-free gate driver and its measured output waveforms [2].

Vertical charge transport via small polaron hopping within lamellar organic single crystal

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Abstract**—**We synthesized tips-pentacene single crystals large enough to enable a two-terminal device operating along the crystals' C-axis. The electric characterization was studied by analyzing the space charge limited current at various temperature and different electric field intensity, and transport mechanism of polaron hopping was confirmed. We utilized appropriate models to successfully simulate the experimental results, and reorganization energy, lattice constant, transfer integral and effective mass have been extracted reasonably. This work may help us deepen understanding the charge transport properties in organic system with a high ordered but strong localized feature.

Keywords—transport; organic single crystal; polaron; space charge limited current (SCLC)

I. INTRODUCTION

Organic semiconductor materials, as the most promising candidates for flexible and large-area electronics products, have been extensively studied for decades. Combined together by much weaker Van de Waals interactions, organic semiconductor transport behavior was quite differently from its inorganic counterpart. Moreover, the softness of the organic materials leads to strong interaction between carriers and molecular vibrations-called local electron-phonon interaction, which allows the formation of polaron and influences charge transport processes greatly.

To study charge transport experimentally, Organic Single Crystals (OSC), as much more ordered systems, are promising for the realization of intrinsic properties of charge transport. Space-Charge-Limited Current (SCLC) has ever been an effective technique to study a semi-conductive single crystal's bulk[1-3].

II. EXPERIMENTAL RESULTS

In this research, we have successfully synthesized an ultra large single crystal of tips-pentacene by employing a modified solution method resorting to a very slow solvent evaporation process. This enables us to realize a two-terminal organic crystalline device. The transport mechanisms of carriers were systematically studied by analyzing the space charge limited currents of the device. Both trap-limited transport[4] and small polaron hopping[5] are employed to analyze the electrical characters of the experimental results.

Current vs voltage relationship was derived from classical Marcus equation and reasonable theories were developed to successfully simulate the experimental data. Values of trap density of states N(E), effective hopping distance a, reorganization energy λ, transfer integral t, effective mass m* were extracted reasonably and fully discussed their physics meaning. We found that hopping transport take places from one molecule to its nearest neighbor alone C-axis, i.e. every molecule acts as a "trap center". This means the small polaron model is more appropriate for the description of transport behavior for the charge carriers along the vertical orientation of the Tips-pentacene single crystal where the transfer integral can be ignore small.

This work may deepen our understanding of the charge transport in well-ordered but strong localized system of organic molecular crystal and help us to optimize the design of organic devices.

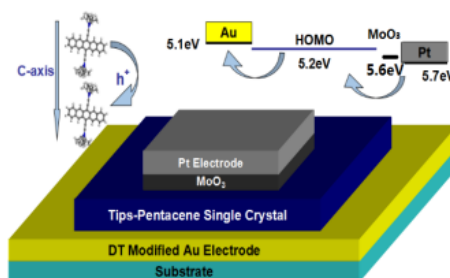

Fig. 1. Schematic of device structure and its band alignment

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INV8-2

Threshold Voltage and Conduction Mechanisms in Disordered Semiconductor-based Thin Film Transistors

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Mobility and Vth extraction by time-of-flight analysis for a-IGZO TFTs

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***Abstract*—We studied time-of-flight (TOF) to extract dynamic carrier mobility (μ_{TOF}) of oxide semiconductor in TFT structure. A negative voltage pulse (V_S) was applied to the source to inject carriers and collect the charges at the drain. The μ_{TOF} was obtained by plotting the transient time (t_{tr}) taken by the carriers to reach the drain against the $|V_S|$. The μ_{TOF} is found to be 24.5 cm^2/V s for dual gate (DG) and 17.6 cm^2/V s for single gate (SG) a-IGZO TFTs.**

Keywords—time-of-flight, a-IGZO TFT, carrier mobility (μ), threshold voltage (V_{th})

I. Introduction

Transient analyses such as time-of-flight (TOF) and charge extraction in a linearly increasing voltage have been used to evaluate the charge carrier mobility or average carrier velocity in TFTs [1]. In this work, μ_{TOF} values for SG-driven and DG a-IGZO TFTs are extracted and compared with μ_{sat} that is extracted by conventional methods [2].

II. Result and Discussion

Fig. 1 (a) shows the transient response of a DG a-IGZO TFT with W of 20 μm and L of 200 μm, for V_S = -5 V. The rectangular trace represents the square-wave input signal and the dotted trace represents the output signal. The delay between the application of the voltage step and the beginning of the current rise is called the "transit time" (t_{tr}) and the rise of the drain current response after this time represents an increasing number of carriers being extracted from the D.

Fig. 2 shows results of t_{tr}^{-1} as a function of $|V_S|$ varied from 5 to 10 V. For both SG-driven and DG-driven a-IGZO TFTs, the data is fitted well by straight lines. However, both fitted lines clearly do not intercept at zero, but at a finite intercept (V_I). Observation of nonzero V_I suggests that the V_{TOF} that pulls carriers across the channel does not equal V_S in the setup but is effectively reduced by V_I [1]. We, therefore, formulate the observation that the V_{TOF} is given by $V_{TOF} = |V_S| - V_I$.

The μ_{TOF} calculated by $\mu_{TOF} = L^2/t_{tr}|V_{TOF}|$ are around 24.5 $cm^2/V{\bullet}s$ for DG a-IGZO TFTs and 17.6 $cm^2/V{\bullet}s$ for SG a-IGZO TFTs. Compared with μ_{sat} from the slope of I_{DS}, which is 15 ± 1 for both DG and SG a-IGZO TFTs, the μ_{TOF} values agree well with the drain current differences between DG and SG a-IGZO TFTs. We also notice that the observed intercepts V_I, around ~3.7 for DG and SG IGZO TFTs, are very similar to the V_{th} of ~3.4 V extracted independently from the conventional saturation curve for both DG and SG TFTs.

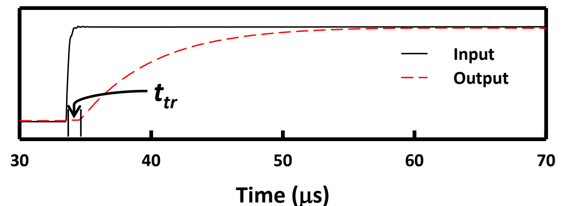

Fig. 1. Oscilloscope screenshot of a a- IGZO TFT for source voltage (V_S) = -5 V.

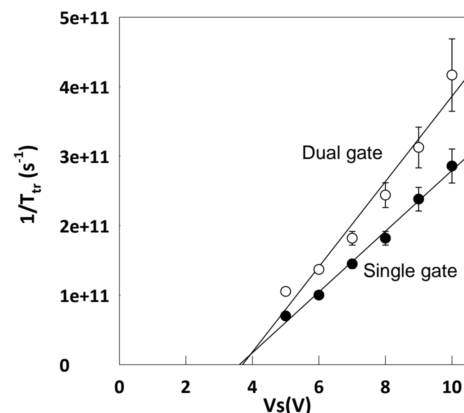

Fig. 2. transient time (t_{tr}) as a function of L^2 for (b) SG-driven and (c) BA a-IGZO TFTs with varying L from 90 to 200 μm.

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Carbon nanotube thin film transistors for display technology

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***Abstract*—As an emerging thin film transistor (TFT) technology, carbon nanotube thin film transistors (CNT-TFTs) have shown high mobility, high on/off ratio and high on-current, which performance may surpass the current TFT technologies. Moreover, the fabrication process is regarded facile, reliable, scalable to large area, and compatible with the current TFT manufacturing process. Thereby, CNT-TFT technology is regarded as a potential candidate for the future flat panel display (FPD) industry, and research on using CNT-TFTs for pixel-driving circuits of display has been performed in many research groups. Active matrix organic light-emitting diode (AMOLED) array driven by CNT-TFTs have been demonstrated in laboratory, which indicates CNT-TFT based backplane is very promising. However, most of the effort on the application of CNT-TFTs for the backplane electronics is in research laboratory, and there are still many challenges before it being commercialized.**

In this presentation, we will report progress on the CNT-TFT technology in our group, and also discuss the challenges from the aspects of the CNT materials production, the fabrication process of the CNT-TFTs, the device performance, stability and uniformity. Though the CNT-TFT technology is not yet ready for backplane production line of FPDs, it arrives at a critical status of being transferred from lab to industry, and the challenges could be overcome by close collaboration between research institutes and FPD manufacturers in the near term.

Keywords—carbon nanotube; thin film transistors; backplane; flat panel display

ACKNOWLEDGMENT

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Low-temperature solution-processed p-type oxide thin-film transistors

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***Abstract*—Solution-processed p-type oxide semiconductors have recently attracted increasing interests for the applications in low-cost optoelectronic devices and low-power consumption complementary metal-oxide-semiconductor circuits. In this work, p-type metal oxide (i.e. Cu_xO and NiO_x) thin films were prepared using low-temperature solution process and integrated as the channel layer in thin-film transistors (TFTs). The electrical properties of the fabricated TFTs, together with the characteristics of oxide thin films, were systematically investigated as a function of annealing temperature. By introducing high-k gate dielectrics, the electrical performance, especially the hole mobility, of devices was improved significantly. Meanwhile, the operation voltage could be reduced to lower than 4 V, which is promising for portable and low-power consumption electronics.**

Keywords—p-type oxides; low temperature; solution process

I. INTRODUCTION

Recently, n-type oxide semiconductor thin-film transistors (TFTs) have received considerable attention due to their excellent electrical performance and high optical transparency in the visible light regime.[1,2] The missing key ingredient for further development of next-generation transparent electronics is their hole-transporting (p-type) counterparts with comparable characteristics, since the latter would enable the development of the much desired complementary metal-oxide-semiconductor (CMOS) circuit architectures. However, there are few works reporting p-type oxide TFTs due to the lack of p-type oxide semiconductors and the difficulty in achieving high-quality p-type film. Compared with vacuum-based techniques, solution process offers additional benefits: simplicity, low cost, high throughput, and the ability to fabricate a wide range of compositions.

II. RESULTS AND DISCUSSION

(1) Solution-processed p-type copper oxide thin-film transistors fabricated by using a one-step vacuum. annealing technique. In this study,[3] copper oxide (Cu_xO) thin films were fabricated on SiO_2/Si substrates by using a solution process. The coated Cu_xO gel films were treated using a vacuum annealing method at various temperatures (400-700 ^oC). With the increase of the annealing temperature, the copper oxide is reduced from CuO to Cu_2O. Meanwhile, the grain size and the root mean square value increase with increasing the annealing temperature. To verify the possible applications of the Cu_xO thin films as channel layers, their applications in TFT devices were demonstrated. These results show that the TFT performance was strongly dependent on the crystallinity and the surface morphology of Cu_xO channel layers. The 600 ^oC-annealed Cu_xO TFT exhibits the best electrical performance, including a high hole mobility of 0.29 cm^2/V s, a small subthreshold slop value of 0.8 V/dec, and a large on/off current ratio of of 1.6×10^4.

(2) Hole mobility modulation of solution-processed nickel oxide thin-film transistor based on high-k dielectric. In this study,[4] we demonstrate the fabrication of solution-processed p-type NiO_x thin films by using monoethanolamine as ionic complex modifier. The high-quality NiO_x thin films were fabricated by thermally decomposing coordination complex ions $[Ni(MEA)_2(OAc)]^+$ at low temperatures. The spin-coated NiOx thin films processed at temperatures lower than 300 ^oC exhibit high transparency (>90%), smooth surface (~0.5 nm), and amorphous nature, which are favourable for large-scale transparent device fabrication. By introducing aqueous high-k Al_2O_3 gate dielectric, the electrical performance of NiO_x TFT was improved significantly compared with those based on SiO_2 dielectrics. Particularly, the hole mobility was found to be 60 times enhancement, quantitatively from 0.07 to 4.4 cm^2/Vs, which is mainly beneficial from the high areal capacitance of the Al_2O_3 dielectric and high-quality NiO_x/Al_2O_3 interface.

ACKNWLEDGEMENT

This study was supported by Natural Science Foundation of China (Grant no. 51472130, 51572135, and 51672142)

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High performance flexible OTFT materials and processes for display, logic and sensor applications

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***Abstract*—High mobility (>4cm2/Vs) p-type organic semiconductor materials are presented suitable for applications in flexible display, logic and sensor fields. The formulation of high k amorphous semiconducting binders with crystalline small molecules produces a formulation that can achieve excellent uniformity of OTFT properties by spin coating.**

Keywords*— *high-k binder; organic transistor; flexible electronics; high mobility

I. INTRODUCTION

Organic transistor technology has improved over recent years and FlexOS™ organic semiconductors currently achieve charge mobility levels of >4cm^2/Vs in short channel (<10 micron) devices over large substrate sizes. NeuDrive Limited, a UK based semiconductor materials company is developing the materials and process technology for generating arrays of devices for flexible displays, logic and sensor devices using established large area manufacturing techniques. The low temperature processes used coupled with the inherent flexibility of organic TFT devices are seen as important for new product concepts with sufficient durability and a cost competitive fabrication process.

II. LOGIC DEVICES

This presentation describes the approach taken to generate logic or display backplane array devices using a 5 mask etch isolation process with minimum feature size of 5 microns. Designs were created using the Process Design Kit (PDK) established at UAB, Barcelona. 5 stage ring oscillators were measured with maximum operating frequencies of 617kHz at 50V (see figure 1). Stage delay for the fastest oscillators were calculated at ~160ns and separate inverter stages were tested at speeds well in excess of 1MHz at 20V peak to peak input square wave waveform. Inverter configurations that produced slower oscillators (f=150kHz) were functional down to 20V operating voltage and it is expected that this could be reduced further through gate dielectric engineering to improve on the relatively low capacitance of these devices (6nFcm^{-2}).

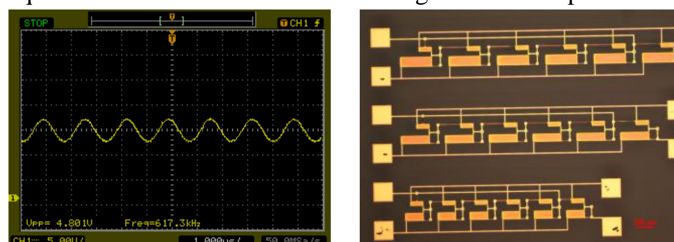

Fig. 1. Output of 5 stage ring oscillator and image of devices

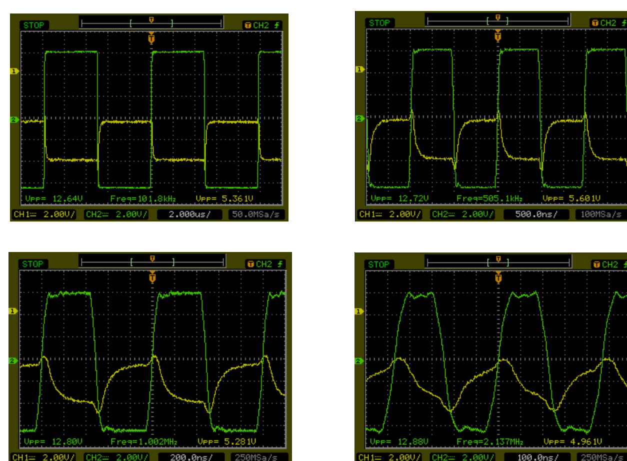

Fig. 2. Inverter output for square wave input of 20V at frequencies of 100kHz (top left), 500kHz (top right) 1MHz (bottom left) and 2MHz (bottom right). Note: output should be scaled by 1.8X to account for the picoprobe impedance mis-match

III. DISPLAY PIXELS

In order to test the suitability of the dry etch isolation process for displays with higher densities we designed TFTs with a size suitable for a 200ppi AMOLED backplane (RGB stripe, bottom emission). TFTs with W/L of 10/4 (design dimensions) were fabricated with high mobility and off currents lower than 0.1pA.

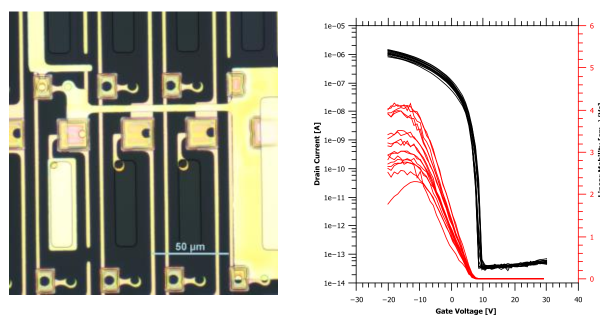

Fig. 3. Image of 2T-1C pixel design (left) and transfer/mobility curve for test element group with W/L of 10/4 microns

On the controversy of carrier mobility in organic TFTs

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Organic thin-film transistors (OTFTs) have achieved remarkable progress in research, showing fast increase in device performance. Recently, the mobility values have been reported to be as high as 40 cm^2/Vs or even to 100 cm^2/Vs [1,2]. However, the mobility extraction method has been questioned and some researchers argue that those "ultra-high" values may not be reliable [3]. Here, we establish the model of resistance network of OTFTs [4-6] and then address the controversy by quantitative modeling and calculations, showing that how the resistance network lead to overestimation of carrier mobility. With this theory, the two segments of the mobility values are well explained (Figure 1a).

In addition, there have been numerous new polymers or small molecules for organic semiconductors. Along with them, researchers have proposed various transport models to predict the temperature-dependent mobility behavior, based on different hypothesis on transport mechanisms [Figure 1b]. Here, we propose that most of models may be generally described by the generalized Einstein relation, based on the mobility-diffusivity relation for non-crystalline or semi-crystalline semiconductors. Within this framework, the different models of temperature- and concentration-dependent carrier mobility may be described as some special cases of the Einstein relation, due to different energetic and structural disorders.

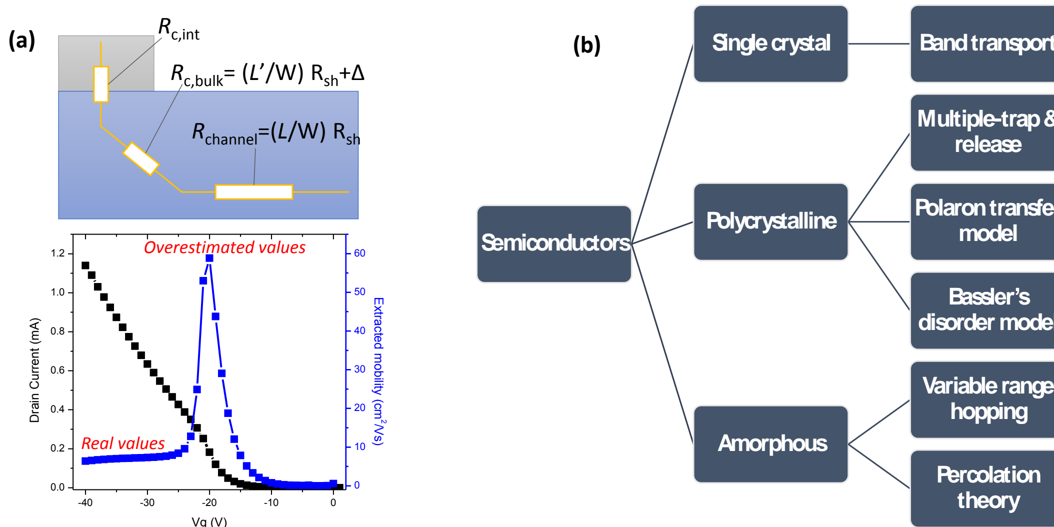

Figure 1 (a) A simulated curve of OTFTs that can lead to overestimation of mobility. (b) Various models for charge transport in organic TFTs that can be described in our theory.

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Printed TFT Logic Circuits

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Abstract—We report the **development of inkjet-printed organic thin-film transistors (OTFTs), inverters and logic circuits on PET substrate. The mobility of 1 cm^2/Vs and 0.1 cm^2/Vs achieved on p-type and n-type printed OTFTs with an operation voltage of 15 V. The printed uniform and thin dielectric layer achieved by introducing coffee ring effect on printing process. A gain value of 24 obtained from the printed CMOS inverter and the device exhibits an excellent air-stability without encapsulation. Our results demonstrated the potential of the developed printed transistors for flexible electronics in the near future.**

Keywords—OTFT, logic gates, CMOS, pinkjet-printing

I. Introduction

Solution proceesable OTFTs attracted a lot of attentions since the last three decades. It's still a challenge to introduce this technology to the commercialization. One of the main challenges is the printing process has a significant impact to the device's performance. The variation between cell to cell is too big and doesn't meet the requirement of mass production. However, the most research groups are using spin coating process for the OTFTs fabrication in order to estimate the performance of materials. It is important to develop the printing process for the fabrication of OTFTs and logic circuits.

II. Experiment Results

A. *Printed thin and uniform dielectric*

Coffee ring effect is usually seen as undesirable characteristics during the printing process, but we propose that the optimization of this effect can lead to thin and uniform printed dielectric layer for OTFTs fabrication. [1] The thickness of dielectric layer can be optimized by changing drop spacing, pixel width and substrate temperature. The roughness of 0.8 nm in the valley area with thickness of 200 nm achieved as shown in Fig. 1. The excellent printed uniformity of dielectric layer enables the fabrication of more complex logic circuits.

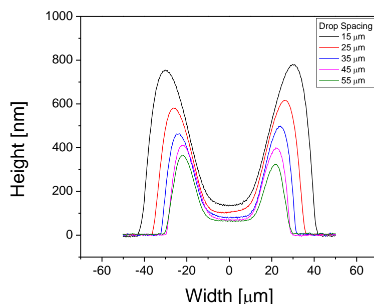


Figure 1. Inkjet-printed dielectric line profile.

B. *3-layer-printed OTFTs with standard deviation of 15%*

Top gate bottom contact OTFTs were fabricated by inkjet-printing method for the deposition of semiconductor, dielectric and silver inks. The device's architecture is shown in Fig. 2. An average hole mobility of 0.9 cm^2/Vs with a relative standard deviation of 15% has obtained from 220 devices.

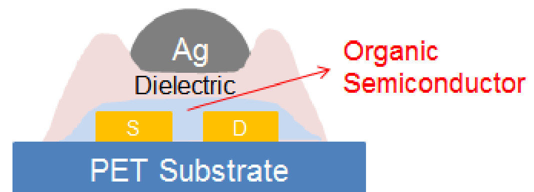
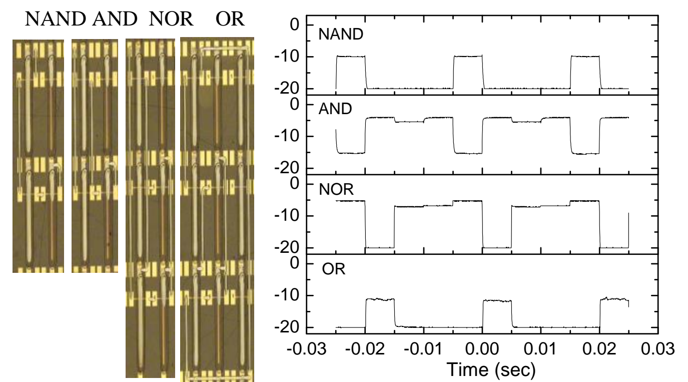


Figure 2. Illustration of 3-layer-printed OTFT architecture

C. *Printed inverters and logic gates*

Four different logic gates (NAND, AND, NOR and OR) were fabricated by the enhancement-load PMOS inverters as shown in Fig. 3. By combine the printed PMOS and NMOS transistors, we also successfully demonstrated a full-swing of CMOS inverter which obtained the gain value of 24 when the supplied voltage at 20 V.



Acknowledgment

The authors would like to acknowledge technical support from Hiroshi Fukutani, Stephen Lang, Eric Estwick, Raluca movileanu, Richard Dudek and Craig Storey. This work was performance as part of the Printable Electronics Program at the National Research Council of Canada.

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Organic Power Electronics: AC-DC Conversion with High-Voltage Organic Thin-film Transistors

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***Abstract*—The control and conversion of electric power, using organic/printable components, aims at further integration of organic electronic systems. With high-voltage organic thin-film transistors, we present AC-DC power converters that enable direct access to power outlets (up to 220 V AC) for powering organic electronic systems.**

Keywords— AC-DC Conversion; High Voltage OTFTs; Power Converters; Rectifiers

I. Introduction

Organic and printed electronics offers a solution for large-are low-cost electronics that can be massively distributed. Printed components, especially transistors with organic/polymer functional materials, suffer from low power efficiency due to the relatively low mobility of charge carriers. The use of organic electronic devices in power applications has been a great challenge. Here, AC-DC converters, comprising organic thin-film transistors (OTFTs), take power from outlets (up to 220 V) and convert the AC voltage to a quasi-constant DC current that can drive other organic functional devices.

II. High-Voltage Organic Thin-Film Transistors

Very few solution-processed OTFTs can survive operation at hundreds of volts, [1] due to the low quality of thin-films comprising defects and pinholes. In this work, solution-processed HV-OTFTs based on polymeric semiconductor poly(3-hexylthiophene-2,5-diyl) (P3HT) together with a 2.5-µm-thick gate dielectric layer of poly(methyl methacrylate) (PMMA) have been developed for high voltage (> 200 V) operation. The maximum drain current at -200 V drain and gate voltages is around 0.7 mA. The mean hole mobility is 2.6×10^{-2} cm^2/Vs and the mean threshold voltage is 2 V.

III. Organic Power Converters

The key of AC-DC conversion is rectifying the input AC voltages. Here, the HV-OTFTs are configured as diodes in both half-wave and full-wave rectifiers to convert high voltage of AC voltages to DC power.

A. Half-Wave Rectifiers

A half-wave rectifier, consisting of one HV-OTFT, one smoothing capacitor (15 µF), and one load resistor (47 kΩ), has been demonstrated as a quasi-constant current supply. [2] The output current is 90 µA at a voltage of 4.2 V, with the load resistance of 47 kΩ. When the load resistance was varied from 10 kΩ to 100 kΩ, the load current decreased slightly from 0.1 mA to 0.08 mA, while the output voltage monotonously increased from 1 V to 8 V.

B. Full-Wave Rectifiers

Similarly, with four diode-configured OTFTs, a full-wave rectifying bridge, as shown in Fig. 1(a), has been implemented. With a load of 47 kΩ and without the smoothing capacitor, the fully-rectified voltage shows peaks of 17.6 V or 19.4 V (red curve in Fig. 1(b)) at 220 V AC input. The DC output current with the smoothing capacitor is 159 µA, while the output voltage is 7.5 V.

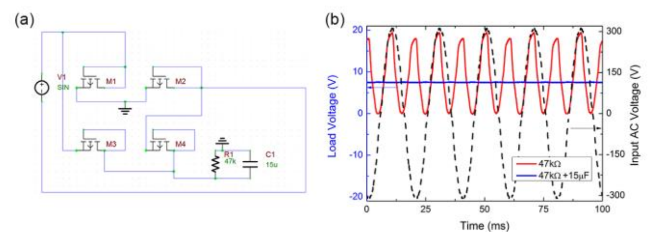

Fig. 1. (a) Circuit schematic of the full-wave rectifier. (b) The rectified output voltage over the load resistor, without (red) and with (blue) a smoothing capacitor connected in parallel with the load. The dashed black line is the input voltage.

Acknowledgment

The authors gratefully thank the Swedish Foundation for Strategic Research for the financial support through the projects “Large-area light-emission on the roll” and “SiOS”, and the Swedish Energy Agency through the MODULIT project in the “Batterifonden” programme.

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High stability of Low temperature and Flexible IGZO TFT by plasma treatment

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***Abstract*—IGZO based flexible TFT was fabricated at low temperature. The performance and stability of the TFT treated with N_2O and NH_3 plasma were studied. The off-state current decreased an order that optimized the electrical properties of TFT. NH_3 plasma treatment is more suitable for TFT processing technology, because of the off-state current can be reduced and the V_{th} can return to positive after the PBTS, NBTS processing technology.**

Keywords—flexible; TFT;IGZO;plasma; low temperture

I. Introduction

Flexible display technology has been an important technology direction of display. Low temperature technology was put forward subject to special restrictions on flexible materials. And IGZO based oxide semiconductor technology is suitable for flexible AMOLED display technology for higher mobility, lower of preparation process temperature, little affected by visible light and can be made into transparent devices, etc. In this paper, low temperature and plasma treatment technology were studied to improve the performance of flexible TFT devices.

II. Experimental Procedure

A bottom gate TFT was fabricated on flexible PI substrate at low temperature. Two samples of the TFT gate insulation layer were treated by N_2O and NH_3 plasma for 10s, respectively. And another sample without any plasma treatments was prepared as contrast. The W/L of TFT is 6um/10um.

III. Results and Discussion

A. I-V curves of flexible IGZO TFT

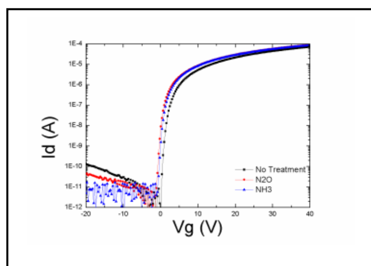

Fig. 1. I-V curves of TFT devives .

Fig.1 shows the I-V curve of flexible IGZO TFT devices under different plasma treatments. V_{DS} was at 10.1V. The V_{th} of no treatment, N_2O plasma and NH_3 plasma treated samples, are at 0.4V, -0.8 V, -0.5V. N_2O and NH_3 plasma decrease the off-state current for an order that optimized the electrical properties of TFT.

B. PBTS and NBTS of flexible IGZO TFT

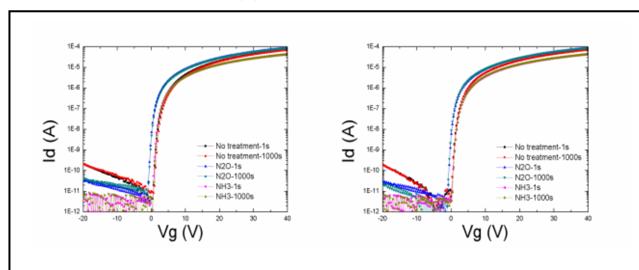

Fig. 2. PBTS and NBTS of TFT devives . (a) PBTS (b) NBTS

Fig.2 shows the PBTS and NBTS of flexible IGZO TFT. V_{th} of NH_3 plasma treated TFT revert to 0.7V and 0.5V under PBTS and NBTS after 1000s. But the Vth of N_2O plasma treated TFT remain at -0.8V regardless of PBTS or NBTS. NH_3 plasma treatment was the optimum process for flexible TFT for the improvement of off-state current, positive V_{th} value and stability of characters in positive and negative bias test. The reason was that the H+ ion filled the Oxygen vacancy of the oxidation silicon gate insulation layer during NH_3 plasma treatment process, and improved the conductive interface state.

Acknowledgment *(Heading 5)*

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Scale-up fabrication of carbon nanotube thin film and its application in thin-film transistors

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***Abstract*—It is desired to produce large-size and high-quality carbon nanotube (CNT) thin film in a cost-effective way for applications in the next generation of flexible electronics. Here, we present a scale-up fabrication method of CNT thin film by a floating-catalyst chemical vapour deposition along with a continuous filtration and transfer system. Thin films, 20 cm in width and no limitation in length, are collected using a continuous-moving membrane filter and transferred from the filter to a polymer substrate by a roll-to-roll method. We also fabricated CNT thin-film transistors, exhibiting a carrier mobility of 42 $cm^2V^{-1}s^{-1}$ and an on/off current ratio of 3×10^5.**

***Keywords*—carbon nanotube; thin film; transistor; scale-up**

I. Introduction

CNTs can be continuously synthesized using an atmospheric-pressure floating-catalyst chemical vapor deposition technique by feeding a carbon source gas with a catalyst precursor. CNT thin films can be collected on a membrane filter by a gas-phase filtration process. However, only single piece of CNT thin films can be obtained, and also the area of thin film is usually limited by the size of membrane filter.[1-2] Here we present a method to fabricate large-area CNT thin film, and further demonstrate the feasibility of its application in thin-film transistors (TFTs).

II. Experiments and Results

As-grown CNTs flowing with carrier gas were deposited onto membrane filter at the end of reaction furnace. Different from standard single piece of filter, a roll of membrane filter was introduced in the continuous filtration and transfer system. The fresh filter was continuously transported in the filtration system, and the filter carried CNTs on it was transported out

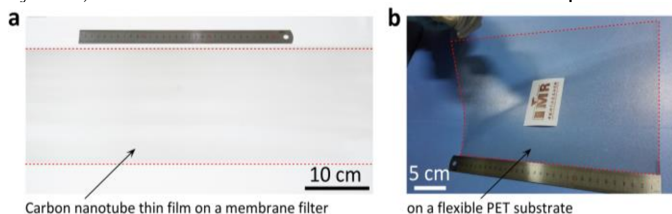

Fig. 1. CNT thin film on a membrane filter (a) and on a PET substrate (b).

of the filtration system, which means that the gas environment is crucial to ensure the gas-flow distributing uniformly at the filtration window, which is achieved by tuning pumping rate. Fig. 1a shows a CNT thin film with 20 cm in width. The nanotube density increases with an increase of the depositing time which can be controlled by adjusting the transfer speed of the filter membrane. Such a nearly free-standing film can be easily transferred from the filter to other substrates. Fig. 1b shows a large-area CNT thin film on a polyethylene terephthalate (PET) substrate by a roll-to-roll transfer method. The film exhibits a sheet resistance of 160 Ω sq^{-1} with optical transmittance of 97% at 550 nm. The low-density CNT films can be used as the channel in TFTs, and electrical performances are shown in Fig. 2. Our results show that CNT thin films are promising for application in transparent conductive films as well as channel and electrodes of TFTs.

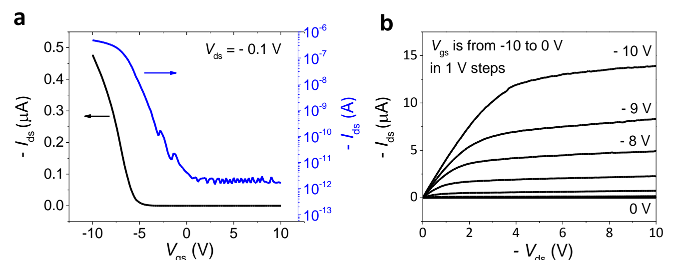

Fig. 2. Transfer (a) and output (b) characteristics of a back-gate TFT.

Acknowledgment

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Current Feedback Driving with Dynamic Supply Voltage Scaling for Low Power AMOLED Displays

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Abstract—the current feedback driving scheme with One-dimensional dynamic supply voltage scaling (DVS) was proposed for AMOLED displays. Simulation results show that this approach can help to significantly reduce the static power, which thus would be a promising way for realizing low power AMOLED displays.

Keywords—AMOLED; low power; current feedback; dynamic supply voltage scaling (DVS)

I. INTRODUCTION

Reducing the power consumption is vital to make active matrix organic light emitting diode (AMOLED) displays to be competitive in mobile and wearable applications. Driving approaches to reduce the DC power dissipated over the driving thin-film transistors (TFTs) have been found to be important [1, 2]. In conventional pixel driver, the driving TFT works in saturation regime to guarantee a constant current flowing through the OLED. As a result, a relative high voltage is needed, though most of the supply voltage drops on the driving TFT, inducing a significant DC power consumption. A current feedback AMOLED driving scheme using 3 TFT and 1 capacitor (3T-1C) in the pixel driving circuit in our previous work, which is able to suppress the influence of non-idealities of TFTs including spatial non-uniformity and temporal variations of the electrical characteristics [3]. It has been proved there's no need for driving TFT to work in saturation region when drive an OLED. Therefore, the supply voltage of pixel driving circuit can be greatly reduced, and lower DC power consumption can be achieved. In the meantime, various dynamic supply voltage scaling (DVS) approaches were also proposed to reduce the power consumption adaptively according to the displayed image, but the reduced power was limited by the high supply voltage of traditional driving scheme [1]. In this work, current feedback driving scheme with one-dimensional DVS was proposed for low power AMOLED displays.

II. METHOD

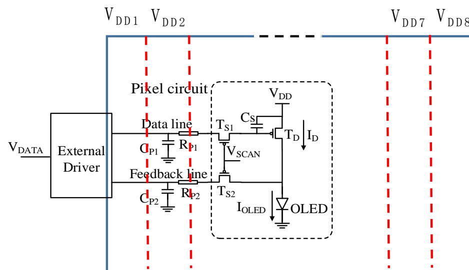

Fig. 1. Illustration of the current feedback driving scheme and the whole display area divided into 8 different column regions with individually adjustable supply voltage (V_{DD}) for dynamic supply voltage scaling (DVS).

As illustrated in Fig.1, the whole display area is divided into 8 different column regions with individually adjustable supply voltage (V_{DD}) for DVS. The pixel circuit is based on the 3T-1C current feedback driving scheme [3]. The simulation was implemented by an in-house built hybrid simulation platform composed of MATLAB and SPICE circuit simulator [1], using p-type poly-Si TFTs with the widely accepted RPI poly-Si TFT model.

III. RESULTS AND DISCUSSIONS

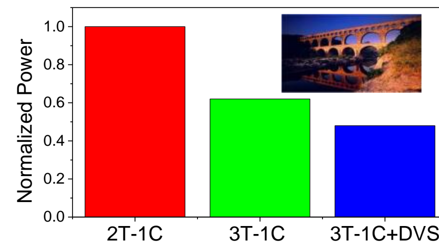

Fig. 2 The simulated power consumption with 3T-1C current feedback driving scheme with and without dynamic supply voltage scaling (DVS). Inset: the image used in the study.

As shown in Fig. 2, for the 3T-1C current feedback AMOLED driving scheme, nearly 40 percent power can be reduced compared to the conventional 2T-1C driving circuit. With DVS technology in 3T-1C driving scheme, the power consumption can be further reduced more than 10%, that is, more than 50% power consumption can be reduced when apply the 3T-1C driving scheme and DVS technology together. Nonetheless, in the interest of time, the power simulation is done with only one test image.

IV. CONCLUSION

In this work, current feedback driving scheme with one-dimensional DVS technology was proposed for AMOLED displays. Simulation results showed that this work significantly reduced the static power in pixel driving circuit, making it a promising way to realize low power AMOLED displays.

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Carbon nanotube thin-film transistors and driving circuits for flexible display application

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***Abstract*—Single-walled carbon nanotube is promising for fabricating flexible thin-film transistors due to its excellent carrier mobility, mechanical flexibility, heat tolerance and low-temperature processing. Here, we report a design, fabrication and performance evaluation of a carbon nanotube thin-film transistor with a photoresist layer as the dielectric, and a 16×16 pixels driving circuit for an active matrix organic light emitting diode display. The single pixel unit demonstrated a hole mobility of 65 cm^2/V^{-1}s^{-1}, an on/off ratio of 10^4 and an on-current of 8 µA.**

Keywords—carbon nanotube; thin-film transistor; driving circuit; display

I. Introduction

Owing to their exceptional properties including electrical conductivity, optical transmittance, mechanical strength and flexibility, carbon nanotubes (CNTs) have attracted great attention for the potential applications in flexible electronics, e.g. driving circuit of an active matrix organic light emitting diode. It is desired to offer a feasible approach to form the insulator or passivation layers of thin-film transistors (TFTs) and circuits, especially for flexible electronics application [1]. Here, we presented an easy method to format the patterned insulator and passivation layers, allowing us to fabricate a driving circuit of 16×16 pixels with CNT network as the channel of TFTs.

II. Device Fabrication and Characterization

Fig. 1 shows the optical images of the fabricated driving circuit, where each pixel includes a switching TFT, a driving TFT and a charge storage capacitor. The buried-gate-type TFTs were fabricated by patterning method of standard photolithography, further covered by passivation layer, and ready for the integration with organic light emitting diodes. CNTs were grown by floating-catalyst chemical vapour deposition (CVD) technique [2]. An insulator layer as well as passivation layer was formed and patterned by a spin-coating of photoresist (Microchem, S1813) and a developing process, and further treated by a heat curing at 150 ℃ for 16 h. The thickness and dielectric constant are evaluated to be 1 µm and 3.42, respectively. Fig. 2 shows the transfer and output characteristics of a single pixel unit. The circuit exhibited the electrical performance of an on/off ratio of 10^4, a mobility of 65 cm^2/V^{-1}s^{-1}, and a driving current of 8 µA, which offers the current high enough to drive the designed organic light emitting diode. It is important that the driving circuit could be operated at the low voltage of less than 10 V even though a 1 µm thick layer was used for the insulator in the TFTs, which is attributable to the sparse CNT network. Finally, our method has been proved to be feasible to demonstrate the flexible driving display.

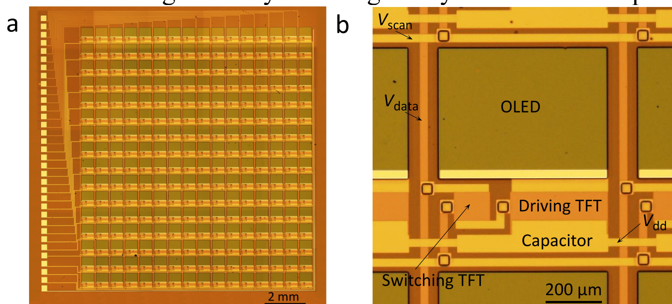

Fig. 1 Optical images of fabricated 16×16 pixels (a) and single pixel unit (b).

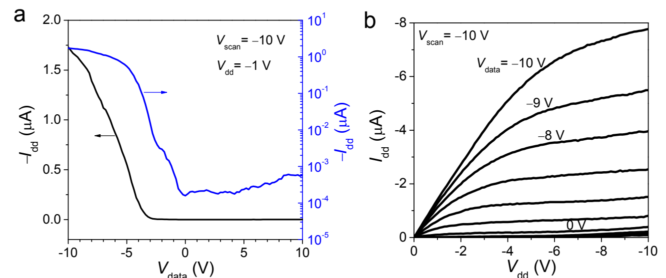

Fig. 2 Transfer (a) and output (b) characteristics of single pixel unit.

Acknowledgment

This work was supported by ‘Flexible electronic devices based on carbon nanotubes’ Fundamental Research Funds for the Central Universities (N130404001), the Project-sponsored by SRF for ROCS, SEM (47-6), National Natural Science Foundation of China (Grants 51272256, 51505304, 61422406, 61574143), Thousand Talent Program for Young Outstanding Scientists.

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Investigation of nitrogen doping and double channel layers for the indium tungsten oxide thin film transistors

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***Abstract*—Oxide TFT has received intensive attention for its excellent performances such as high mobility, large area uniformity, high transparency and low cost. It may be utilized in the flexible, 3D and transparent display technologies. It is reported that tungsten doping has a special influence on the oxide TFTs [1-3]. We investigated the nitrogen doped indium tungsten oxide TFTs by adding nitrogen gas during the sputtering process. XRD analysis proves that all the films are amorphous and AFM measurement confirms that the films show smooth surface. The transmittance in the visible light region (380 - 780 nm) is above 85%, which is favorable in practical devices. With the nitrogen flow rate increases from 0% to 3%, 5%, 6%, the threshold voltage shifts from -8.5V to -5.5V, -0.5V, 9.5V, indicating that nitrogen doping can suppress the carrier concentration, thus leading to the threshold voltage positive shift. Due to fewer carriers, the device mobility drops a little, but still above 20 $cm^2V^{-1}S^{-1}$. When the nitrogen flow rate is 5%, the TFT shows the optimized performance with the threshold voltage of -0.5 V, field effect mobility of 24.44 $cm^2V^{-1}S^{-1}$, on/off current ratio of 1×10^7, and subthreshold swing of 0.38 V/decade.**

Figure 1 shows the dependency of transfer characteristic curves of the TFTs with single a-IWO:N channel layer on the different nitrogen flow rates. The thickness of channel layer is 10 nm deposited by radio frequency magnetron sputtering method. The channel width of 1000 μm and length of 250 μm were defined by a shadow mask. We fixed the working pressure and change the nitrogen flow rate during the sputtering process to obtain different nitrogen doping ratio. The IWO target with ratio of indium oxide to tungsten oxide of 98:2 (wt.%) was used. Source and drain electrodes with thickness of 50 nm were prepared using ITO target at sputtering power of 50 W. At last, all the devices were treated by thermal annealing at 100℃ in nitrogen atmosphere for half an hour. Obviously, the transfer curves shift positively and the optimized performance is obtained at nitrogen flow rate of 5%.

We further fabricated the TFTs with a-IWO/a-IWO:N double channel layers to investigate the influence of double layer on the electrical performance and stability of the devices. The results demonstrate that threshold voltage of the TFTs with double layers shift less than that of the single layer in measurement conditions under positive gate bias stress, positive gate bias temperature stress, negative gate bias stress, and negative gate bias temperature stress test. The deposition procedure of the a-IWO and a-IWO:N layer can also influence the electrical stability effectively, since double layer TFTs with a-IWO:N deposited on a-IWO perform better than the TFTs with inverse procedure. We think that when a-IWO:N were deposited on the IWO layer, it may act like the passivation layer, protecting the device from influence of atmosphere on the backchannel surface, leading to the better electrical stability.

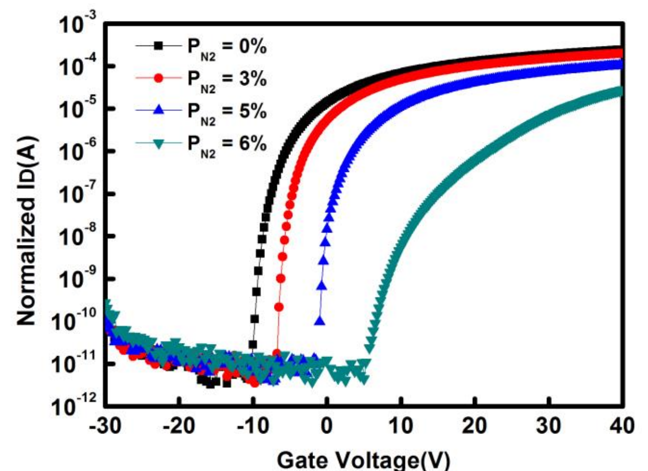

Fig. 1. Dependency of transfer characteristic curves of the TFTs with single a-IWO:N channel layer on the different nitrogen flow rates.

Key words—a-IWO; nitrogen-doping; double channel layer; thin film transistors

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Ultra-High Mobility Thin-Film Transistors with MOCVD Growth In_2O_3

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So far, a-IGZO TFTs have stably achieved mobility larger than 10 cm^2/Vs, but it is still unable to compete with low temperature poly-silicon (LTPS) TFTs (50-100 cm^2/Vs). It is insufficient to match any high frame rate display such as high performance AMOLEDs or system-on-panel (SoP) applications. The field-effect mobility of TFTs with pure In_2O_3 channel is probably the highest for the In-Ga-Zn-O system [1]. However, In_2O_3 is an intense degenerated semiconductor. The background carrier density easily reaches 1×10^{18} to 1×10^{19} cm^{-3} even in un-doped In_2O_3, resulting in large off-state current or even the incompetence of realizing off-state. In this work, In_2O_3 channel layer was deposited by metal organic chemical vapor deposition (MOCVD), which is supposed to be one of the simplest techniques for the growth of high-quality films with an advantage of producing uniform, reproducible, and adherent films. In addition, oxygen microwave plasma treatment was applied to the In_2O_3 channel layer to reduce the background carrier density. The field-effect mobility of In_2O_3 TFTs was achieved as high as 243 cm^2/Vs.

The schematic cross sectional structure of the In_2O_3 TFTs is shown in Fig. 1 (a). An 100-nm-thick silicon dioxide (SiO_2) gate dielectric was grown by thermal oxidation on the back gate electrode of heavily doped n-type silicon (100) substrate. Then, a 15-nm-thick In_2O_3 channel layer was grown on the SiO_2 gate dielectric by MOCVD. The source/drain (S/D) electrodes with a stack structure of indium tin oxide (ITO) and aluminum (Al) were deposited by radio-frequency (RF) magnetron sputtering and e-beam evaporation, sequentially. Finally, the In_2O_3 channel layer was treated by O_2 microwave plasma for various times at room temperature.

As shown in Fig. 1(b), for In_2O_3 TFTs without O_2 microwave plasma treatment (0 min), the transfer curve showed almost the same conductivity regardless of the change of V_{GS}. The In_2O_3 TFT worked as an unadjustable resistor. It can be explained that there is too high background carrier density in the as-deposited In_2O_3 channel layer. After the O_2 microwave plasma treatment, the typical transfer characteristics of TFTs were obtained. A positive shift of V_{on} was observed as the plasma treatment time increases, indicating that the carrier densities of the channel layers decrease with increasing plasma treatment time. In addition, the on-state drain current reduced when the plasma treatment time increased to 30 min, revealing the lower μ_{FE} of TFTs. Figure 2 (a) shows the I_{DS}-V_{GS} transfer curves with various V_{DS} for the In_2O_3 TFT treated by O_2 microwave plasma for 20 min. The on/off current ratio of the TFT was about 10^7 and the sub-threshold swing (S.S) was 0.7 V/decade. The linear (V_{DS}=100 mV) mobility were estimated from Fig. 2 (b) as high as 243 cm^2/Vs.

In order to further investigate the effects of O_2 microwave plasma treatment, the carrier densities, chemical characteristics, and surface potential of In_2O_3 channel were measured by Hall Effect measurement, XPS spectra and KFM, respectively. The results indicate that the plasma treatment made a considerable increase in the chemisorbed oxygen, which is due to the O ions adsorption on the In_2O_3 surface. The oxygen ions adsorption results in the depletion of the In_2O_3 channel from its surface. As a result, with the plasma treatment time increased, the carrier densities decreased from 1.6×10^{19} cm^{-3} to 2.4×10^{17} cm^{-3}.

In this study, the μ_{FE} of the In_2O_3 TFTs was estimated as high as 243 cm^2/Vs, which is regarded as the highest μ_{FE} among that of the oxide semiconductor TFTs reported until recent year. Both their transport mechanism and electronic structure are carefully analyzed also.

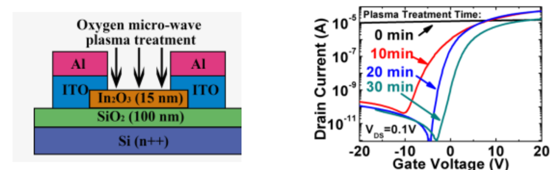

Fig.1 (a) Schematic cross section of the In_2O_3 TFT with bottom-gate structure, and (b) I_{DS}-V_{GS} transfer curves in liner regime (drain voltage = 0.1 V) for In_2O_3 TFTs with various time of O_2 microwave plasma treatment.

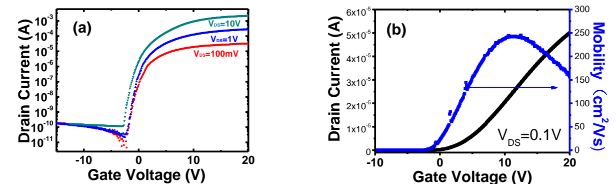

Fig.2 For the In_2O_3 TFTs treated by O_2 microwave plasma for 20 min: (a) I_{DS}-V_{GS} transfer curves in different V_{DS}. (b) The linear mobility as a function of V_{GS}.

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Reduction of Leakage Current by Wet Anneling on BLA Polycrystalline Silicon Thin-Film Transistor

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***Abstract*— In this study, the H_2O plasma wet annealing is proposed to reduce the leakage current of polycrystalline silicon (poly-Si) TFTs. By comparing the insertion of without and with wet annealing step into the TFT fabrication process, the continually increased gate leakage currents without wet annealed TFTs were effectively suppressed by wet annealing and maintained the current of 10^{-13}A.**

Keywords—Polycrystalline silicon (p-Si), thin-film transistor (TFT), blue laser annealing (BLA), low temperature polycrystalline silicon (LTPS).

I. Introduction

In active matrix display, low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) are widely employed because of the high field effect mobility above the 80cm^2/Vs. And to form the LTPS, excimer laser annealing (ELA) had been conventionally utilized to many of commercial products. However, ELA has the problem that very high cost of manufacturing and maintenance. Also, high leakage current is remained as the further works. In this work, the LTPS were formed by using blue laser annealing (BLA) as we developed previously [1]. And the wet annealing process steps into the TFT fabrication were employed to reduce the leakage current.

II. Result and Discussion

P-type LTPS TFTs with conventional top gate structure TFT is fabricated as shown in figure 1 (a) and (b). The amorphous silicon was crystalized by using BLA. Then after, we insert the intermediate annealing step with two different ambient that dry N_2, which is generally used, and H_2O plasma wet annealing, which are proposed. Moreover, when after device fabrication finished, the post annealing condition was also kept with the intermediate annealing condition.

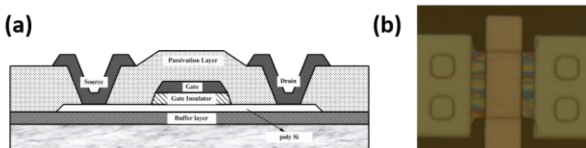

Fig. 1. (a) Schematic cross-sectional view of BLA-TFT, (b) image of TFT

The transfer characteristics were measured as shown in figure 2 that V_{DS} is (a) -0.1V, (b) -1V and (c) -5V. It is obviously appeared that the black line of dry N_2 annealed LTPS TFTs exhibited high leakage current. In contrary, the wet annealed LTPS TFTs exhibited lower leakage current as indicated by red lines. Therefore, the insertion of wet annealing is technique to reduce the leakage current of LTPS based TFTs.

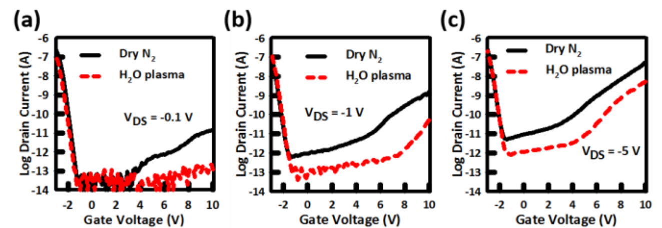

Fig. 2. (a),(b) and (c) are leakage current at VDS of -0.1, -1, -5V. The TFT's channel width W = 20 μm and channel legnth L = 8 μm

III. Conclusion

The formation of LTPS by using BLA with H_2O plasma wet annealing as intermediate process step into LTPS TFT process is proposed. The leakage current was effectively reduced, resulting in less than 10^{-13}A.

Acknowledgment

This research was supported by BK21 PLUS, the MOTIE (Ministry of Trade, Industry & Energy (10052044) and KDRC (Korea Display Research Corporation) support program for the development of future devices technology for display industry. This work was supported by the BK21 Plus Program (Future-oriented innovative brain raising type, 21A20130000018) funded by the Ministry of Education (MOE, Korea) and National Research Foundation of Korea (NRF).

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The Applications of OECTs in Supercapacitor Balancing Circuits

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***Abstract*— In this paper, we investigate using OECTs in differential amplifiers and cell voltage equalizers for supercapacitor balancing circuits. The differential amplifier based on OECTs can sense voltage difference and the voltage equalizer consisting of a microcontroller and OECTs can be used to charge supercapacitors to desired voltages.**

Keywords*— Organic electrochemical transistors, differential amplifier, supercapacitor balancing, printed electronics

I. Introduction

OECTs are based on PEDOT:PSS as the active material and are printed on a flexible plastic sheet using screen printing. Differential amplifiers and shunt transistors have a key role in the balancing circuits monitoring, controlling and balancing the charge between several storage cells. This work shows how OECTs can be used in both differential amplifiers and shunt transistors.

II. OECT-based Differential amplifier

Printed organic electrochemical transistors printed at Acreo AB and discrete resistors were used to build a differential amplifier on a breadboard. The schematic of the circuit is shown in the inset on the right side of Fig 1. A fixed voltage of 1.1 V is applied to the first input, and the second input is swept twice, first from 0.5 to 1.7 V and then reverse. The gain of the amplifier can be increased by adjusting the resistor values. The hysteresis effect seen in Fig 1. is related to memory properties of OECTs. It is reduced at slower sweeps.

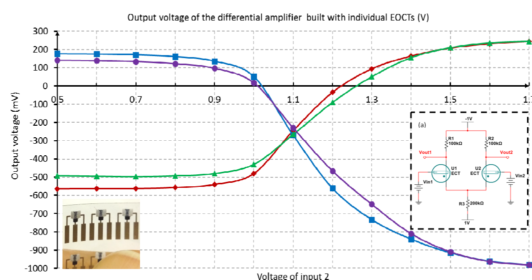

Fig. 1. Transfer characteristics of the two outputs of the differential amplifier. The left inset shows the printed OECTs and the other inset is the circuit schematic. The red and blue curves are Vout1 and Vout2 respectively, for the ascending sweep and the green and purple curves in the descending sweep.

III. Hybrid balancing circuits

In this experiment, the microcontroller senses the voltages across the two capacitors (intentionally imbalanced), and turns the OECTs on as soon as the voltage across each capacitor reaches 1 V. The two voltage dividers are utilized to obtain the desired V_{GS}=1 V, relative to the source of each transistor from the digital outputs of the microcontroller.

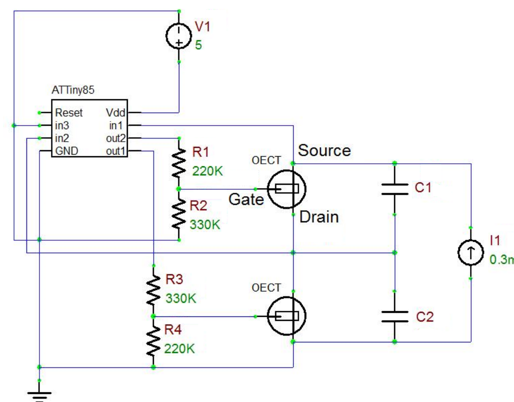

Fig. 2. Circuit diagram of the OECT-based balancing circuit that balances the two unbalanced capacitors.

Acknowledgment

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A Fluorescence Detector for Rapid On-Chip Detection of Amniotic Fluid Embolism Biomarker Based on Dual-Gate Photosensitive Thin-Film Transistor

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Amniotic fluid embolism (AFE) is a rare and fatal obstetric medical condition occuring during delivery. Maternals' lives could be in danger as quickly as in a few minutes when encountering AFE. Thus, early detection and treatment become extremely critical. To achieve effective and reliable early detection, one promising approach is to frequently monitor relevant biomarkers of AFE contented in blood in a real-time fashion. Doctors are given sufficient time and early precaution to conduct an emergency treatment if the content of biomarker in blood reaches a set threshold or presents an aggressive content-increasing trend. As far as a biomarker is concerned, Zinc Coproporphyrin I (ZnCP-I) in blood plasma is proven to be well correlated with AFE and can be potentially used by detecting its induced fluorescence (Fig. 1A) [1]. However, its current detection method, namely laser-induced fluorescence together with high-performance liquid chromatography is often time-consuming, costly, and requires complex optical systems.

In this work, we propose a compact microanalytical system (Fig. 1B) for rapid fluorescence detection of ZnCP-I where a high-brightness LED is used as a light source, a microfluidic chip separating ZnCP-I from blood sample, an optical filter that blocks excitation light from LED and lets only fluorescence pass through to the detector below, and a dual-gate a-Si:H photosensitive thin-film transistor (DGTFT) (Fig. 2A) working as a direct fluorescence detector. To achieve efficient low-level fluorescence detection, a three-dimensional DGTFT will be designed to attain both efficient light absorption and fast switching characteristics, as shown in Fig. 2B. In addition, the DGTFT will work in the subthreshold region to achieve high sensitivity and low noise. We anticipate that this detection system can be potentially integrated with current blood samplers, to form a point-of-care platform for blood testing during delivery, and achieve high sensitivity, acceptable detection limit, and wide dynamic range.

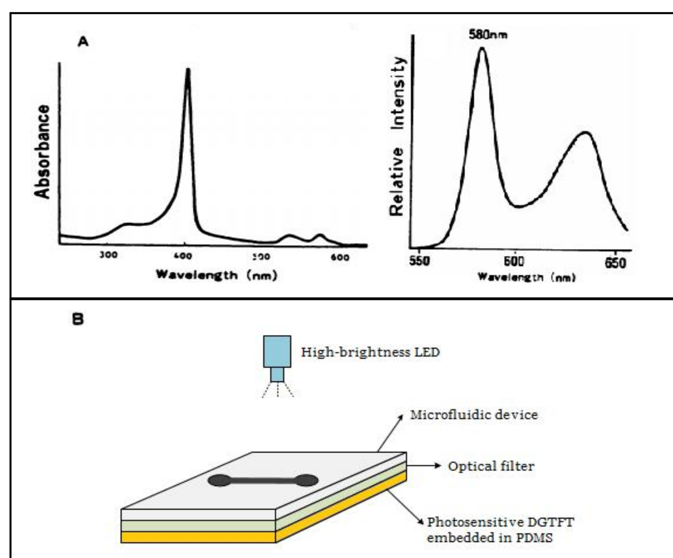

Fig. 1. (A) Absorbance spectrum (left) and fluorescence spectrum (right) of ZnCP-I[1]. (B) A cross-sectional view of the proposed microanalytical system for rapid detection of ZnCP-I.

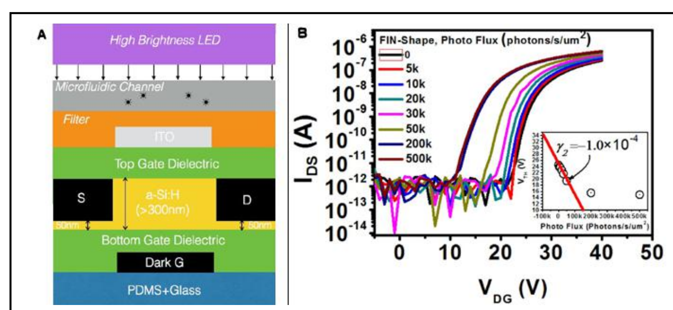

Fig. 2. (A) Cross-sectional structure of DGTFT-based fluorescence detector. (B)Transfer characteristics of the three-dimensional FIN-shape DGTFT under different photo flux of light exposure.

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Printed Thin-film Transistors and Circuits Based on Sorted Semiconducting Single-walled Carbon Nanotubes

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***Abstract*—in this report, we developed a valid approach to sort large-diameter semiconducting single-walled carbon nanotubes (sc-SWCNTs) from commercial SWCNTs using new organic conjugated compounds and achieved more than 10 high-performance printable sc-SWCNTs inks. Print TFT arrays and simple logic gates and circuits based on sorted sc-SWCNTs were obtained on rigid and flexible substrates. Printed TFTs exhibited low operating voltage, small hysteresis, high mobility and on/off ratios. Furthermore, printed circuits also showed good performance.**

Keywords—printable electronics; sorted semiconducting carbon nanotubes; thin-film transistors, circuits

I. Introduction

Printed thin film transistors (TFTs) are the core elements to construct various printed devices and systems, including backplanes for displays, printed logic gates and circuits, biologic and chemical sensors, and artificial electronic skin. Performance of printable semiconductor inks is critical for high-performance TFTs. Sc-SWCNTs have been become a promising semiconductor for printed TFTs, especially for flexible printed TFTs, since SWCNTs show excellent electrical properties, solubility, flexibility, high chemical and physical stability, and process temperatures compatible with flexible substrates.[1-3]

II. Experimentals

Arc discharge SWCNTs were dispersed in 15 mL solvents containing a certain amount of different polymers via probe-ultrasonication for 30 min (Sonics & Materials Inc., Model: VCX 130, 60W). Then, the resulting SWCNT solutions were centrifuged to remove metallic species and big bundles, and sc-SWCNT inks (Figure 1a) were directly used to fabricate SWCNT TFTs and simple circuits. To achieve top-gate SWCNT TFTs onto the PET substrates, sorted sc-SWCNT inks were selectively deposited on device channels, followed by washing with toluene for 3 times. The procedure was repeated 3 times. After that, HfO_2 thin films were deposited on top of pre-deposited SWCNT thin films by ALD. Then, silver top-gate electrodes were printed on the top of ALD HfO_2 thin films by aerosol jet printing. Printed top-gate TFTs were integrated to circuits with printed silver lines. The electrical properties of TFTs were measured at room temperature.

III. Results and Discussions

As shown in Figure 1b, printed CMOS inverters exhibited low operating voltage, small hysteresis, high voltage gains and noise margins. Flexible CMOS inverters exhibited large noise margin of 84% at low voltage (1/2 V_{dd}=1.5 V) and maximum voltage gain of 30 at V_{dd} of 1 V. Both of the noise margin and voltage gain are one of the best values reported for flexible CMOS inverters at V_{dd} less than 1.5 V. A 3-stage ring oscillator has also been demonstrated on PET substrates and the oscillation frequency of 3.3 kHz at V_{dd} of 1 V is achieved.

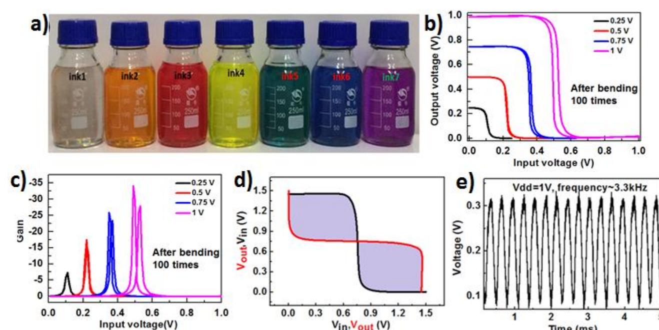

Figure 1 a) Optical images of printed sc-SWCNT inks, b-d) printed CMOS inverters and e) a 3-stage ring oscillator.

Acknowledgment

This work was supported by Natural Science Foundation of China (91123034, 61102046), Strategic Priority Research Program of the Chinese Academy of Science (XDA09020201), the Knowledge Innovation Programme of the Chinese Academy of Sciences (KJCX2-EW-M02), Basic Research Programme of Jiangsu Province (BK2011364) and Basic Research Programme of Suzhou Institute of Nanotech and Nano-bionics (Y5AAY21001).

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Solution-Processed High-k Magnesium Oxide Dielectric for n-Type In_2O_3 and p-Type NiO Thin Film Transistors

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***Abstract*—In this work, magnesium oxide (MgO) dielectric films were fabricated using a low-cost spin-coating method. The as-prepared MgO dielectric films annealed at various temperatures (400, 500, 600, and 700℃) were characterized by using Thermogravimetric analysis, X-ray diffraction, atomic-force microscope, optical spectroscopy, and a serious of electrical measurements. In order to validate the application of MgO thin film as a gate dielectric, the n-type indium oxide (In_2O_3) and p-type nickel oxide (NiO) channel layers were separately fabricated on optimized MgO dielectric layer. The n-type In_2O_3 TFT exhibited an electron mobility of 4.8 cm^2 V^{-1} s^{-1}, an on/off current (Ion/Ioff) ratio of 10^7, and a subthreshold swings (SS) value of 0.33 $decade^{-1}$. The p-type NiO TFT showed a hole mobility of 2.81 cm^2 V^{-1} s^{-1}, an SS value of 1.49 $decade^{-1}$, and an Ion/Ioff of 10^3. It is noted that all these parameters were obtained at a low operation voltage of 6 V, which represents a great step toward the achievement of low-cost, all-oxide, and low-power consumption CMOS devices..**

Keywords—spin-coating method; high-k dielectric; thin-film transistor;

INTRDUCTION

Along with the rapid development of display technology, high-speed, low-cost displays become one of the growing trends. However, majority of TFTs employ conventional dielectric material, e.g., SiO_2, which usually results in high operation voltage due to its weak capacitive coupling between the gate electrode and active channel. To address this issue, high-k dielectrics have been widely investigated in metal-oxide-semiconductor TFTs to achieve low-voltage operation due to high permittivity than SiO_2 (k=3.8). High-k dielectrics possess potentials to increase the physical thickness of the dielectric and to make the capacitance density unchanged. Beside, low power consumption is one of the key issues for the mobile applications, due to the limit capacity of the rechargeable lithium-ion battery. To date, MgO thin films have been prepared by using various vacuum-based techniques, such as electron-beam evaporation, and high-pressure sputtering, which can result in higher processing costs and incompatibility with substrates. In contrast, solution processing usually exhibits benefits such as simplicity, atmosphere processing, and low fabrication cost. Moreover, the surface morphology of the annealed films fabricated by solution-processed is smoother. In this work, the MgO thin films were deposited via solution-processed method, which offers the attraction of low-cost and high-throughput advantages. Therefore, thin film formed by solution-processed is a key method for next-generation TFTs.

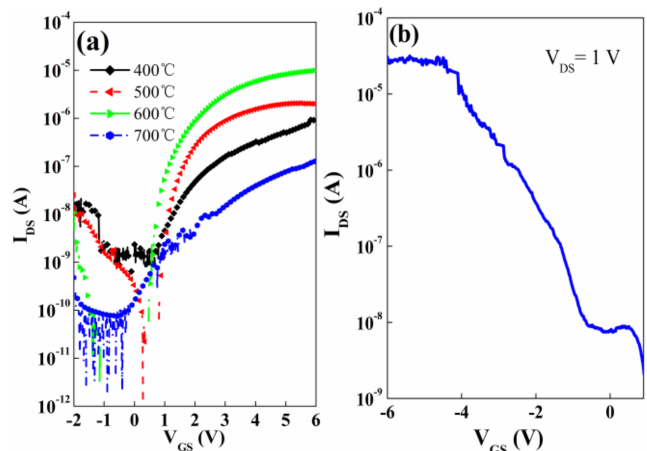

Fig. 1. (a) Transfer curves of In_2O_3 TFT with MgO dielectrics anneal ed at various temperatures. (b) Transfer curves of NiO/MgO TFT.

ACKNOWLEDGEMENT

This study was supported by Natural Science Foundation of China (Grant no. 51472130 and 51572135) and Natural Science Foundation of Shandong Province (Grant no. ZR2012FM020).

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Artificial Neural Network Compact Model for TFTs

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***Abstract*—This paper reports a TFT compact modeling methodology based on artificial neural networks (ANNs). Both drain current and gate capacitance are modeled. The required data is generated by Silvaco Atlas.**

Keywords—Compact model; TFT; Neural network;

I. Introduction

Thin-film transistors (TFTs) have important applications in various microelectronic, such as active-matrix organic light-emitting diode (AMOLED) display. To enable quality design of TFT backplanes, circuit-level simulation (such as SPICE) is indispensable, which demands accurate and efficient compact models of TFTs. Deriving physics-based compact models for TFTs, however, is a challenging task, due to the fact that the device physics have not been completely understood, some are even under debates. This makes physics-based modeling a time-consuming process and less capable of adapting to the specific technologies of different device makers.

In this work, we propose to use artificial neural networks (ANN) to construct compact models for TFTs. There are several advantages of using ANN-based compact modeling in replace of conventional compact models: 1) **One needs not know all the underlying physics when forming the ANN.** The ANN model will "automatically learn" the inherent physical pattern from the training data. This is particularly suitable for emerging devices, whose physical models are highly complicated and analytical expressions are difficult to arrive. Adaption to different manufacturers' technology is also easier with the black-box nature of ANNs; 2) The resulting ANN compact model automatically satisfies the **smoothness** requirements for the nonlinear solution of circuit simulation, with **infinite differentiability.**

II. ANN-Based TFT Compact Models

An ANN is a multi-layer interconnected network. See Fig. 1 for a typical three-layer ANN in which the nodes are called neurons. An activation function (sigmoid etc) and a bias are associated to each neuron and a weight is associated to each link. Once the topology is determined, the ANN is mainly characterized by its weights and biases, which are determined in the training process with a specific training algorithm and pre-obtained input-output data. With sufficient neurons an ANN can approximate ANY continuous function, however nonlinear it may be (the universal approximation theorem).

The ANN compact model in this work takes in the bias parameters, such Vgs and Vds, and the device parameters, such as channel length L and width W, and outputs the predicted drain current Ids and the gate-source capacitance Cgs, as shown in Fig. 1. The ANN model can readily used in SPICE-like simulators. The evaluation efficiency depends on the size of the ANN, but is generally comparable with traditional compact models as the ANN evaluation involves mainly vectorized functional evaluations

III. Numerical Experiments

We simulate IGZO TFTs with different W/L ratios in Silvaco Atlas to generate the data required to train and test the ANN compact model. The geometry parameter space are L = [10,15,20,25,50] μm, W = [10,25,50,100,200,500,1000] μm, leading to 35 devices. The Ids and Cgs are measured at Vgs = [0:1:15] V, and Vds = [0:1:16] V. Advanced physical models such Fermi statistics and universal Schottky tunneling are included to guarantee the physical relevance.

All the coding is done in Matlab. The ANN structure is selected to be [10,10,10] (3 hidden layers each with 10 neurons). To train the ANN, we select the I-V and C-V curves corresponding to the crossover points of the W-L grid formed by L = [10,20,50] and W = [10,50,200,1000] as the training data (12 devices), and the curves for L = [15,25] and W = [25,100,500] (8 devices) as the validation data. The curves for the remaining 15 devices are used to test the trained ANN. The training algorithm is trainbr with MSE performance metric.

The comparisons between ANN and the simulation results with the testing devices (not known to the ANN) are shown in Fig. 2 – 4. The good fitting accuracy demonstrates the generalizability of the ANN model. The voltage-dependent capacitance, which involves quite complicated physical mechanisms, is also captured to a reasonable accuracy.

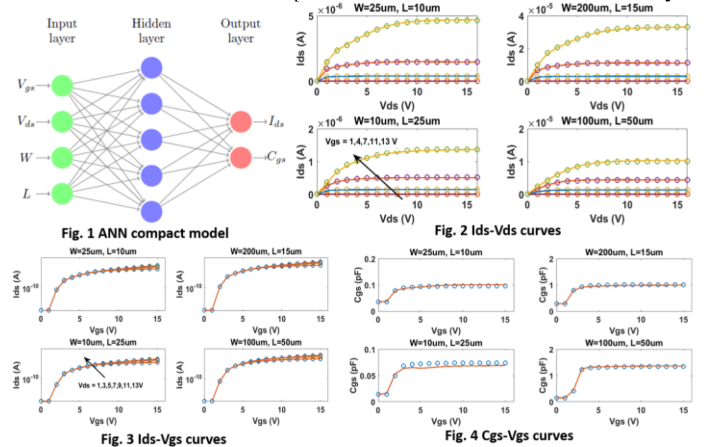

Fig. 1 ANN compact model

Fig. 2 Ids-Vds curves

Fig. 3 Ids-Vgs curves

Fig. 4 Cgs-Vgs curves

The Description of Pinch-off Point for Short Channel Organic Thin Film Transistors

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***Abstract*—We present a comprehensive description of the pinch-off point in organic thin film transistors (OTFTs) originating from space charge limited current conduction. More narrowly, based on the physical pinch-off point expression, a channel-length modulation model is proposed, and it covers all regimes of OTFTs operation, linear and saturation. Especially, getting rid of the influence of the contact resistance, the abnormal output curves for low drain voltage can be well described. For DNTT transistors with channel lengths of 5um and 1um, the Source-Drain currents show excellent agreement with the proposed model.**

Keywords—Organic thin film transistors (OTFTs), Short channel effects, Pinch-off point, Space charge limited current (SCLC).

I. Introduction

In earlier years, several models had have been described the electrical properties of OTFTs with short channel [3-5]. On the one hand, based on the models evolving from traditional silicon-based metal oxide semiconductor field effect transistors (MOSFETs), they showed high accuracy when provided with correct parameters. However, the difference of charge transport mechanism and device structure, limits the application of MOSFET model to organic device. On the other hand, based on the variable range hopping model, the super linear output curves, as well as non-saturating current, can be adequately described. Nevertheless, the site of pinch-off is ambiguous and the influence of parasitic contact resistance is not considered in the previous model.

II. Experiment

The heavily p-doped silicon substrates with thermally grown oxide 100 nm thick SiO_2 was used as the gate dielectric. For figure 1(a), Bottom contact source and drain electrodes with a channel width of 1mm and channel lengths of 1, 2, 5, 10, 20um were fabricated on the oxide surface using lift-off photolithography. The channel length is determined by KFM, like figure 1(b). The electrical characteristics of the fabricated devices were measured by a Keithley 4200-SCS semiconductor characterization system in a clean and shielded box at room temperature in air.

III. Conclusions

The model is presented here that larger material disorder and permittivity and smaller dielectric layer thickness will contribute to the increasing of the source drain currents. In addition, the super linear output characteristic curves were ascribed to contact resistances for short channel OTFT at low drain voltage.

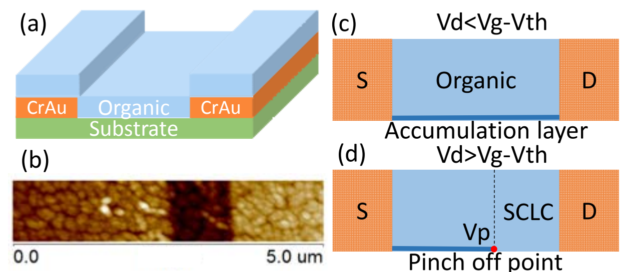

Fig. 1 (a) cross-sectional schematic view of the fabricated OTFTs, (b) AFM image of OTFTs with near 1um channel length, (c) modes of operation in the linear regime, and (d) in the saturation regime.

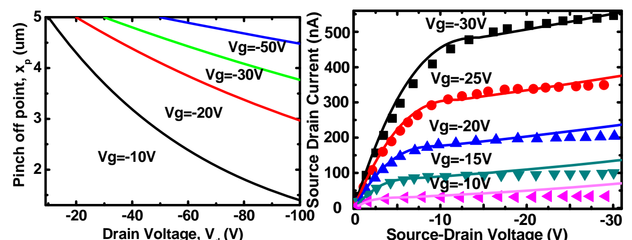

Fig.2. (a) the site of pinch off point at different gate and drain applied bias, (b) the output curves fitted with our model for OTFT with 5um channel.

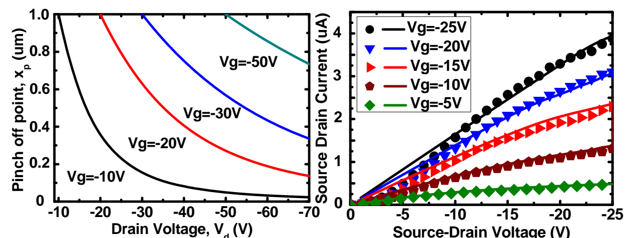

Fig. 3 (a) the site of pinch off point at different gate and drain applied bias, (b) the output curves fitted with our model for OTFT with 1um channel.

Acknowledgements

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Physical Modeling of AOS TFTs Based on Symmetric Quadrature Method Considering Degenerate Regime

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***Abstract*—Explicit analytical solutions to the surface potential and current of amorphous oxide semiconductors TFTs are presented. By reformulating Lambert function as two different exponential terms in different cases, we avoid much of the complexity that degenerate induces. Symmetric quadrature method is adopted here. The model shows a good agreement with the experimental data and is suitable for circuit simulations.**

Keywords—amorphous oxide semiconductor thin film transistors; degenerate conduction; Symmetric Quadrature Method.

I. INTRODUCTION

Amorphous oxide semiconductor has been emerged as a prime candidate for the next generation TFTs technology. Thus an accurate physic-based model of these devices is desperately in need. Notably, the conduction band edge of amorphous oxide semiconductors is composed of spherical overlapping orbitals, which results in the density of band tail states is 2 or 3 orders of magnitude lower than amorphous silicon [1]. Degenerate conduction is occurred and Fermi-Dirac statistics must be employed to develop a model that reflects the physical fact.

II. ANALYTICAL DC I-V MODEL

A. Surface potential calculation

The free charge concentration n_{free} and the trapped charge concentration n_{trap} can be expressed as[2]

$$n_{free}(\varphi,\phi_n)=N_c 2\sqrt{2}W_0\left[R_0\exp(\varphi/\phi_t)\right] \tag{1}$$

$$n_{trap}(\varphi,\phi_n)=g_c\theta_t\left\{2\sqrt{2}W_0\left[R_0\exp(\varphi/\phi_t)\right]\right\}^{T/T_t} \tag{2}$$

where R_0=exp((-ϕ_n+ϕ_{f0})/ϕ_t)/$2^{1.5}$. Since in non-degenerate case, Boltzmann approximation is still valid, and in degenerate case, Lambert function can be simplified as another exponential term. The total value of surface potential is obtained as

$$\varphi_s=\frac{1}{m}\ln\left(\frac{1}{1/\exp\left(m\varphi_{s_str}\right)+1/\exp(m\varphi_{s_sub})}\right) \tag{3}$$

φ_{s_sub} and φ_{s_str} are the band bending in different regions, they can be derived by neglecting n_{free} and n_{trap} respectively .

B. Drain current solution

Substituting (1) and (2) into the Poisson's equation, the surface electric field can be derived and thus the accumulation charge Q_{ac} is approximated as

$$Q_{ac}\simeq q\frac{2\sqrt{2}N_cV_tW_0\left[R_0\exp(\varphi/\phi_t)\right]}{\sqrt{F_1(\varphi,\phi_n)+F_2(\varphi,\phi_n)}} \tag{4}$$

$$F_1=\frac{G_fW_x}{4+2W_x},\quad F_2=\frac{G_t\left(2T_t-T\right)^2W_x^{\frac{T}{T_t}}}{4T_t^2\left[1+TW_x/\left(T+T_t\right)\right]^{\frac{2T_t-T}{T}}} \tag{5}$$

where $G_f=2^{5/2}N_cq\phi_t/\varepsilon_s$ and $G_t=2^{1+3T/2Tt}g_c\theta_tq\phi_{trap}/\varepsilon_s$. W_x refers to $W_0[R_0\exp(\varphi/\phi_t)]$. We adopt symmetric quadrature method proposed in[3], and finally find drain current as

$$I_{ds0}=\mu_{FE}\frac{W}{L}\left[\left(4Q_{am}+Q_{as}+Q_{ad}\right)\Delta\varphi/6+Q_{as}V_t-Q_{ad}V_t\right] \tag{6}$$

Here $\Delta\varphi=\varphi_{sd}-\varphi_{ss}$, Q_{as} and Q_{ad} are the accumulation charges at source and drain respectively. To calculate Q_{am}, one needs W_x at the potential midpoint, i.e. W_{sm}. For an explicit result, W_{sm} can be roughly expressed as

$$W_{sm}=\left(W_{ss}+W_{sd}\right)/2 \tag{7}$$

W_{ss} and W_{sd} refer to W_x at source and drain respectively.

III. RESULTS AND DISCUSSION

A sample of IZO TFT with the structure shown in Fig.1 has been measured. The fabrication process is briefly described as follow: DC sputter devoted Al electrode and gate insulator generated through the anodization process. A 30nm IZO film was deposited by RF magnetron sputtering. SiO_2 and Mo electrode were formed by PECVD and sputtering respectively.

Fig.2 and Fig.3(a) show the comparisons of drain current between model(lines) and experimental data(makers). Fig.3(b) depicts the transconductance characteristics for V_{ds}=0.1V. Obviously, the proposed model gives an accurate description for a wide range of gate and drain voltages.

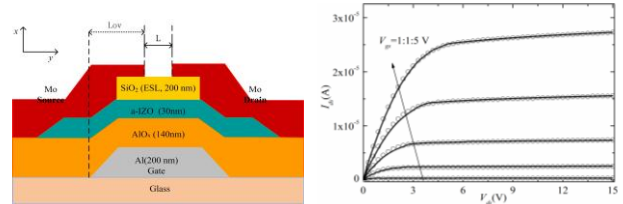

Fig.1. The structure of a IZO TFT.

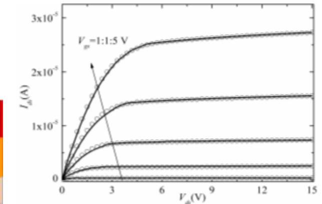

Fig.2. Comparison of output I-V curves.

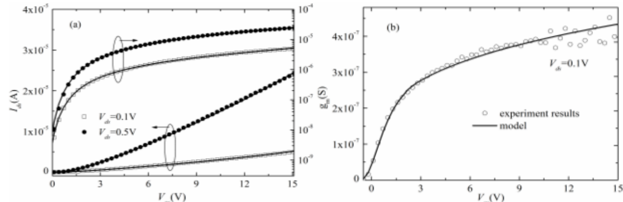

Fig.3. Comparison of (a) transfer characteristics and (b) transconductance .

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Improved Bias Stress Stability for Low-voltage Polymer OTFTs with Low-k/High-k Bilayer Gate Dielectric

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***Abstract*—Low-voltage solution-processed organic thin-film transistors (OTFTs) were developed using a large permittivity (high-*k*) polymer P(VDF-TrFE-CFE). It was shown that by inserting a thin, low-polar dielectric layer (CYTOP) between the high-*k* one and the channel, the bias stability was much improved due to screening of the dipole field from high-*k* dielectric.**

***Keywords*—Organic thin fim transistor (OTFT); low voltage; stability; bilayer dielectric**

I. Introduction

Recent developments in the field of organic thin-film transistors (OTFTs) have led to an increasing interest in achieving a low-operating voltage for the envisioned portable or wearable applications. Thus solution-processed high permittivity (high-*k*) dielectric materials, which are compatible to low-cost high throughput printing processes, have attracted considerable attention. However, carrier localization in the channel could be enhanced at the high-*k* dielectric surface, resulting in mobility degradation. [1] Moreover, the resulted instability is also a potential issue for OTFTs with higher-*k* gate dielectrics. This work shows by inserting a low-*k* polymer dielectric layer between the high-*k* one and the channel, the bias stress stability can be significantly improved.

II. Experimental

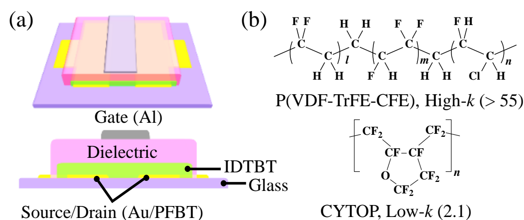

Fig. 1. (a) Schematic of the fabricated OTFT structure and (b) molecular structures and permittivity values of the used polymer dielectric materials.

OTFTs in top-gate bottom-contact structure were fabricated as shown in Fig. 1(a). Cr/Au source/drain electrodes were firstly thermally evaporated to define a channel width of 2000 μm and a channel length of 120 μm, and then treated with pentafluorobenzenethiol (PFBT) before deposition of channel layer. IDTBT in chlorobenzene solution was spin-coated, followed by annealing at 150 ℃ for 30 mins, to form the channel. About 8 nm thick CYTOP and 270 nm thick P(VDF-TrFE-CFE), with their molecule structures shown in Fig. 1(b), were deposited subsequently by spin-coating to obtain the bilayer gate dielectric. Finally, aluminium (Al) gate electrodes were deposited by thermal evaporation with shadow mask.

III. Results and Discussions

As shown in Fig. 2, even with smaller gate dielectric capacitance, the bilayer gate dielectric OTFT exhibits higher ON current and thus larger ON/OFF current ratio, since the low-*k* layer can effectively screen the dipole effects from the high-*k* one and thus minimize the carrier localization to remain high mobility. [1] The bias stress stability is also significantly improved. The high-*k* only device presents a large threshold voltage (V_{th}) shift after a continuous negative gate voltage bias stress for one hour, while negligible V_{th} is found with the bilayer dielectric device.

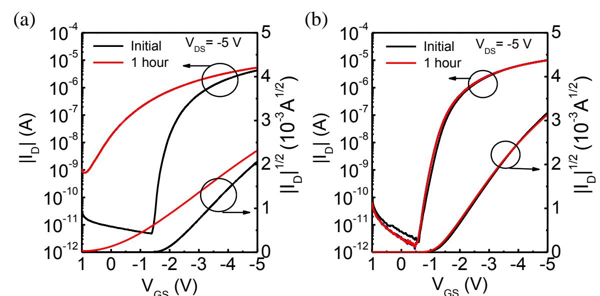

Fig. 2. Transfer characteristics of OTFTs with (a) P(VDF-TrFE-CFE)-only and (b) CYTOP/P(VDF-TrFE-CFE) bilayer dielectric, respectively, under negative bias stress (NBS) (V_{DS} = -0.5 V, V_{GS} = -5 V).

IV. Conclusions

High-k/low-k bilayer gate dielectric was introduced to fabricate low-voltage solution-processed IDTBT polymer OTFTs. The inserted low-*k* CYTOP is proved to provide a fine semiconductor/dielectric interface for higher mobility and improved bias stability by screening of the dipole field from the high-*k* layer. These findings highlight the importance of using high-*k*/low-*k* bilayer gate dielectric for developing high-performance stable low-voltage OTFTs.

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Nitrogen Doping Amorphous InGaZnO Thin Film Transistors for Highly Stable Operation Under Gate Bias and Light Stressing

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Recently, the amorphous InGaZnO thin film transistors (a-IGZO TFTs) received wide attention as they potential applications in high resolution display, flexible display and wearable devices. However, threshold voltage (V_{th}) shift under gate bias, light, or thermal stress is some of the challenging issues in its commercialization. Nitrogen *in-situ* doping in a-IGZO channel has been reported as a suggested way to improve stability of a-IGZO TFTs[1, 2]. Moreover, the shortcoming of nitrogen doping is its undesirable effect on narrowing optical bandgap of a-IGZO film[3], which may deteriorate reliability against negative gate bias and light stress.

In this study, we systematically discuss the role of nitrogen doping on stability of a-IGZO TFTs by fabricating channel layer by RF sputtering in various kinds of atmosphere. The inverted staggered a-IGZO TFTs structure were used in this paper. The nitrogen doping was performing during active layer depositing by *in-situ* injecting nitrogen into the chamber. As shown in figure 1(a)-(c), we compared stability of three kind of TFTs with active layer deposited at Ar/O_2 (20:20), Ar/N_2 (30:1) and $Ar/O_2/N_2$ (30:0.5:0.5) atmosphere. Compared with the other two, the a-IGZO TFTs with active layer deposited at $Ar/O_2/N_2$ atmosphere exhibit good stability under various kind of stress.

To probe the role of nitrogen atom in a-IGZO TFT stability, we used XPS analysis to study the chemical bondings in a-IGZO films. The O 1s spectra of different kinds of a-IGZO film was shown in figure 2(a)-(c). The XPS results confirm that the N atom is more effective than the O atom in suppressing the formation of oxygen vacancies. Moreover, with more nitrogen atoms, the peak position of O_{vac} is found to shift towards a higher binding energy (~0.3 eV) and it indicates that, apart from the overall numbers, the ionic binding of oxygen vacancies has also been changed. Different from previous studies, we purposed that the incorporation nitrogen atom in a-IGZO film will turn origin type oxygen vacancies into two new type oxygen vacancies, which reduce its sensitivity to oxygen adsorption and enhance PGBS stability. On the other hand, we also avoid the NBLS stability deteriorated by depositing a-IGZO film under $Ar/O_2/N_2$ atmosphere.

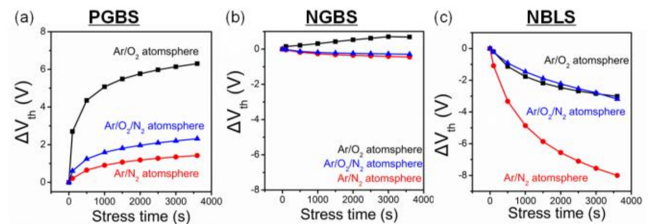

Fig. 1. The $\Delta V_{th}(t)$ of diffferent a-IGZO TFTs under (a) PGBS, (b) NGBS and (c) NBLS.

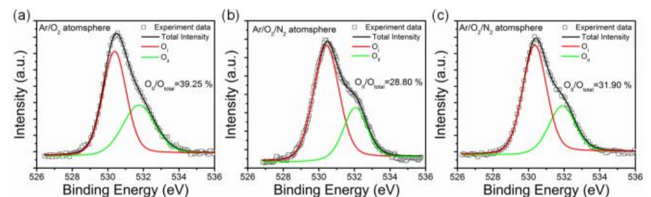

Fig. 2. The O 1s spectra of a-IGZO film deposited under (a) Ar/O_2 atmosphere, (b) Ar/N_2 atmosphere, and (c) $Ar/O_2/N_2$ atmosphere.

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Ambient effects on the light illumination stability of amorphous InGaZnO thin film transistors

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***Abstract*—The light illumination stability of amorphous InGaZnO thin film transistors (a-IGZO TFTs) under various ambient gases was investigated, where oxygen and moisture were proved to be responsible for the improving effect of the ambient air on the light illumination stability of a-IGZO TFTs.**

***Keywords*—Amorphous InGaZnO (a-IGZO); Thin film transistor (TFT); light illumination stability; Ambient gas.**

I. Introduction

Amorphous InGaZnO (a-IGZO) thin film transistors (TFTs) have been considered as one of the most promising candidates to drive next-generation displays. The ambient gases were reported to play an important role on the light illumination stability of a-IGZO TFTs [1, 2]. However, how exactly the components of the ambient air, mainly referring nitrogen, oxygen, moisture, and inert gases, affect the light illumination stability of a-IGZO TFTs still remains unclear so far.

II. Experiment procedure

The inset of Fig. 1 (a) shows the schematic cross section of the passivation-free inverted-staggered a-IGZO TFT used in this study. The transfer characteristics of the devices were measured in an unsealed probe station chamber. The argon, nitrogen, oxygen, and moisture (along with Ar) could be injected into the chamber directly. The photo excitation was provided by a xenon light source in combination with a mono-wavelength generator and an optical fiber.

III. Result and discussion

Fig. 1 (a) shows the transfer characteristics of the a-IGZO TFTs exposed to different light illumination under ambient air. The threshold voltage (V_{th}) shifted negatively and the drain current (I_{on}) increased a little with the light illumination increasing. Fig. 1 (b) shows the ΔV_{th} of a-IGZO TFTs as a function of light illumination under ambient air, argon and nitrogen respectively. Here we regarded the transfer characteristic of the devices under the ambient argon as a reference. The light illumination dependence of ΔV_{th} under the ambient air indicated that air could apparently improve the light illumination stability of a-IGZO TFTs. Besides, the similar tendency could be observed with the case under the ambient argon, implying that nitrogen could hardly interact with the back channel of the devices.

Fig. 1 (c) shows the ΔV_{th} of a-IGZO TFTs as a function of light illumination under ambient oxygen with low, middle, and high content respectively. With the oxygen content increasing, much smaller V_{th} reductions were observed because the ambient oxygen suppressed the oxygen vacancy generation and the oxygen desorption between back channel and environment.

Fig. 1 (d) shows the ΔV_{th} of a-IGZO TFTs as a function of light illumination under ambient moisture with low, middle, and high content respectively. With the moisture content increasing, much smaller V_{th} reductions were also observed, probably owing to the fact that the ambient moisture could assist suppressing the oxygen desorption during the light illumination tests.

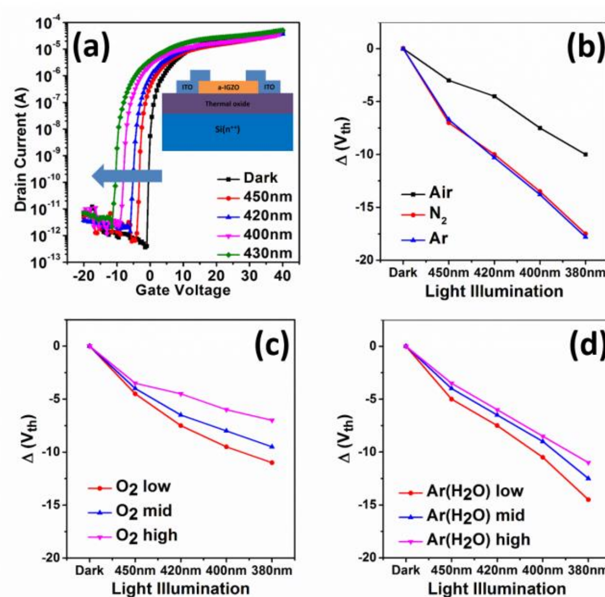

Fig. 1. (a) Transfer characteristics of the a-IGZO TFTs exposed to different light illumination under ambient air. Light illumination dependence of ΔV_{th} for the a-IGZO TFTs under (b) the ambient air, argon, and nitrogen respectively, (c) different oxygen contents, and (d) different moisture contents.

Acknowledgment

This work was supported by National Natural Science Foundation of China (Grant No. 61136004, 61474075).

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Noise Margin Analysis for Pseudo-CMOS Circuits

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***Abstract*—Despite the large noise margin merit of pseudo-CMOS logic, its analytical model is absent. In this paper, we derive the static noise margin model for pseudo-CMOS (pseudo-D) logic circuits. Finally, we analyze the impact of design parameters on noise margin. Simulations show the modeling error is about 3%.**

Keywords—TFT logic circuits, pseudo-CMOS, noise margin

I. INTRODUCTION

Most TFT technologies only have unipolar devices. To improve the noise margin (NM) of unipolar circuits, the pseudo-CMOS logic [1] was proposed, where pseudo-D structure is shown in Fig. 1. However, it is unfavorable that the analytical NM model for pseudo-CMOS logic is absent. In this paper, we derive the NM model for pseudo-D logic circuits based on single-V_{th} TFT which covers the parameters of threshold voltage (V_{th}) and size of TFT, and supply voltage (V_{DD} and V_{SS}). Based on that, we analyze the impact of design parameters of the circuits (the TFT size and V_{DD}) on the NM.

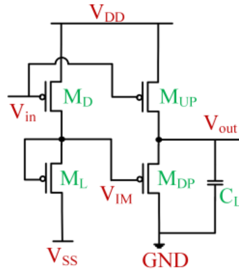

Fig. 1. The schematic of pseudo-D inverter.

II. NM DERIVATION

In pseudo-CMOS inverter, the left two TFTs constitute a zero-V_{GS} load inverter and its NM has been derived [2]. Therefore, taking V_{SS} into consideration, and assume N_1 is the size ratio of M_D to M_L, the output of 1st stage, V_{IM}, can be written as follows.

When $0 \le V_{in} \le V_{in,a}$,

$$V_{IM} = V_{in} - V_{th} + \sqrt{(V_{DD} + V_{th} - V_{in})^2 - N_1 V_{th}^2}\ , \quad (1)$$

and when $V_{in,b} \le V_{in} \le V_{DD}$,

$$V_{IM} = V_{ss} + V_{th} - \sqrt{V_{th}^2 - (V_{DD} + V_{th} - V_{in})^2 / N_1}\ , \quad (2)$$

We assume that the states of M_D and M_L changes at $V_{in,a}$ and $V_{in,b}$. The results can be calculated as follows.

$$V_{in,a} = V_{in,b} = V_{DD} - (\sqrt{N_1} - 1)V_{th}\ ,$$

$$V_{out,a} = V_{DD} - \sqrt{N_1} \cdot V_{th}\ ,\ V_{out,b} = V_{th} + V_{SS}\ .$$

The right two TFTs also form an inverter which be analyzed with similar method to the left. Note that the states of M_{UP} and M_{DP} change simultaneously with M_D and M_L. Accordingly, we can get the equations of 2nd stage as follows.

When $0 \le V_{in} \le V_{in,a}$, M_{UP}/M_{DP} is in linear/ saturation region.

$$V_{out} = \frac{1}{N_2+1}(V_{in} + N_2 V_{IM} - N_2 V_{th} - V_{th}) + \frac{1}{N_2+1}\begin{pmatrix} (V_{in} + N_2 V_{IM} - N_2 V_{th} - V_{th})^2 - \\ (N_2+1)[N_2(V_{IM} - V_{th})^2 - V_{DD}(V_{DD} - 2V_{in} + 2V_{th})] \end{pmatrix}^{0.5} . \quad (3)$$

When $V_{in,b} \le V_{in} \le V_{DD}$, M_{UP}/M_{DP} is in saturation/linear region,

$$V_{out} = V_{IM} - V_{th} + \sqrt{(V_{IM} - V_{th})^2 + (V_{DD} - V_{in} + V_{th})^2 / N_2}\ , \quad (4)$$

where N_2 is the size ratio of M_{UP} to M_{DP}.

With (1) to (4), we obtain the numerical solution of NM.

III. VALIDATION OF DERIATIONS

We adopt the HSPICE LEVEL 40 HP a-Si TFT model for simulation. V_{SS} is set to $-V_{DD}$ and N_2 is set to 2. The results of output voltage curve (VTC) and the NM under different N_1 and V_{DD} are given in Fig. 2. Our models are consistent with the simulations and the average error of NM is only about 3%.

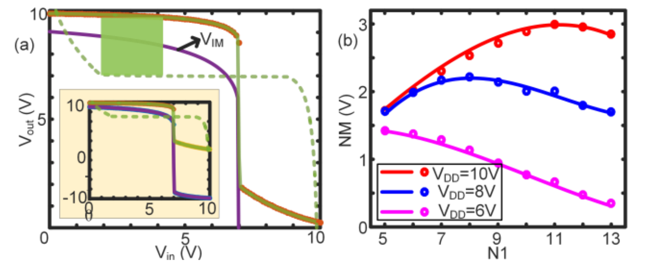

Fig. 2. (a) The VTC and (b) the NM of simulation and calculation resluts.

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Technology Independent Yield-Aware Place & Route Strategy for Printed Electronics Gate Array Circuits

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***Abstract*— We present a new Placement and Routing (P&R) strategy for implementing digital Organic/Flexible/Printed Electronics (PE) circuits based on an Inkjet-configurable Gate Array (IGA) design style together with digital printing personalization.**

***Keywords*— Organic/Flexible/Printed Electronics; Place & Route; physical design; layout; EDA; CAD; digital circuits; Inkjet Gate Arrays.**

I. Introduction

In this work, we present a Place & Route (P&R) strategy for PE designs, addressing an Inkjet-configurable Gate Array [1] design style together with digital printing personalization. Our approach is able to abstract from fabrication details and maximize the yield at circuit level, out of variable mid-yield foils from distinct technologies. We also cope with intrinsic properties and issues of PE circuits, between different technologies and even between individual foils (or chips) of the same technology, because their yield and failure distribution can vary. The yield-aware strategy we propose herein produces the correct wiring (or drop) information to implement the desired circuitry by taking as input the position of all working OTFTs characterized in a previous step, also known as Known Good Organic transistors (KGOs).

II. Place & Route Considerations

The typical modus operandi of P&R algorithms can be divided in two stages: (1) to apply a constructive algorithm to build an initial feasible solution of the problem; and (2) to iterate over that initial solution optimizing a concrete (set of) objective(s) until it reaches a good-enough state or cost function. A review on Placement algorithms can be found in [2]. Further P&R techniques for Gate Arrays and Standard Cell design styles can be found in [3].

Modern EDA tools (commercial, free, open-source, academic…) cover mostly Standard-Cell VLSI placement for CMOS design style. Our approach is oriented to a Gate Array design strategy, dealing with the P&R over pre-designed wire tracks. One of the limitations of PE technologies is that we cannot consider over the cell routing (sea-of-gates) due to the limited stack of layers (as opposed to modern VLSI).

III. Place & Route Strategy

We propose to partition the IGA template into configurable Basic Bulk Cells (BBCs). These BBCs are composed by a specified number of Drive and Load PMOS OTFTs. Gates coming from minimized gate-level circuit netlists (as the ones from [4]) are mapped onto the IGA template designs through these BBCs depending on the KGOs distribution, and the availability of the wire tracks and connectivity zones.

The Placement and Routing is done in a joint process since the placement itself occupies tracks along the wire cells, both locally (inside each BBC) and globally (between BBCs). The strategy is to identify the connectivity zones, which are layout objects of the IGA templates. These objects correspond to I/O pads, characterization pads of the OTFTs, vias (as tracks or holes to be filled by droplets), etc., depending on the targeted technology. If the KGO map allows building a selected gate in any given BBC then the placement of each of its OTFTs is done by filling those connectivity zones with the layer associated to the metal that customizes it by digital printing. The wire tracks of the BBC are being occupied as the placement progresses. Once a BBC doesn't have any more space for placing remaining gates an adjacent BBC is selected to continue the P&R, while keeping the information of the nets that have to be connected globally (connections between logic gates) and the location of the tracks they occupy.

Finally we obtain the complete layout of the interconnections.

Since the KGO varies from foil to foil, the powerfulness of our approach relies in the fact that we can run our algorithm as many times as required for every specific PE circuit after its testing, thus allowing its individual wiring, what maximizes yield at circuit level.

Acknowledgment

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Design Methodology for a Fingerprint Sensor-Integrated Display Pixel and Array based on Dual-Gate a-Si:H Photosensitive TFT

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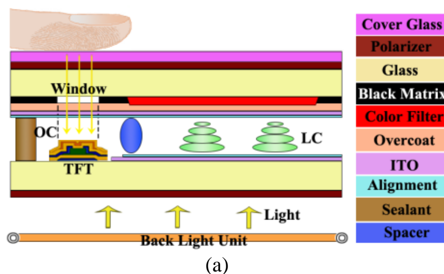
***Abstract*—This paper aims to provide a design methodology for fingerprint-sensor-integrated display pixel and array based on dual-gate photosensitive amorphous silicon (a-Si:H) thin-film transistor (TFT).**

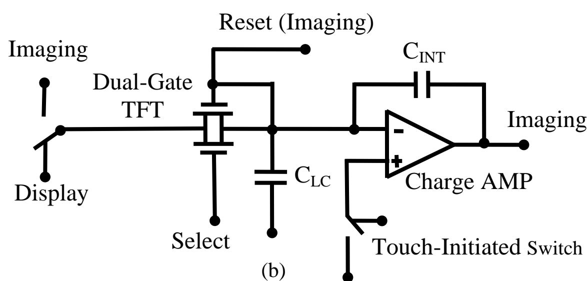
***Index Terms*—Dual-gate TFT; a-Si:H; fingerprint sensor; active matrix liquid crystal display**

With increasingly demands on mobile security and friendly user interface, a fingerprint sensor that can recognize a user's identity becomes ubiquitous and widely accepted. Currently, almost all mobile devices with fingerprint authentication unanimously utilize a discrete fingerprint sensor located either in the area of "home" button or on the back cover. We have proposed an integrative approach to a fingerprint sensor embedded in a display pixel [1, 2].

Illustrated in Fig. 1. (a), such a pixel captures an image of fingerprints in real time through operation of a dual-gate a-Si:H photosensitive thin-film transistor (TFT), offers a high-resolution dynamic fingerprint identification and leads to a high security. The pixel operates in either display or imaging mode with using a touch-initiated switch as seen in Fig. 1.(b).



(a)



(b)

(a) The schematic diagram of fingerprint-sensor-integrated display pixel ; (b) Its circuit functioning in both display and imaging modes.

The dual-mode operation brings a challenge to pixel design. This work will focus on a design methodology of such a fingerprint sensor-integrated display pixel and array. Under the guidance of liquid crystal driving's theoretical design principle, fig. 2. (a) plots the storage capacitance as dependence of designed channel width to meet the requirement of driving a high-resolution display pixel of 264 μm×264 μm with 88% fill factor in the case of 6 μm channel length. With the computer-aided calculation, the channel width has to be designed in the range of 25~30 μm. To meet the requirement of an optical sensor, the pixel design should consider both noise and sensitivity. The analysis shows that the number of noise electrons will be increased with increasing channel width while the sensitivity defining as the ratio between photo current and dark current is independent with the channel width and length as shown in Fig. 2. (b).

Under this methodology, we will further design, fabricate, and evaluate a small 128 × 128 sensor array to enable fingerprint-sensor-integrated display applications.

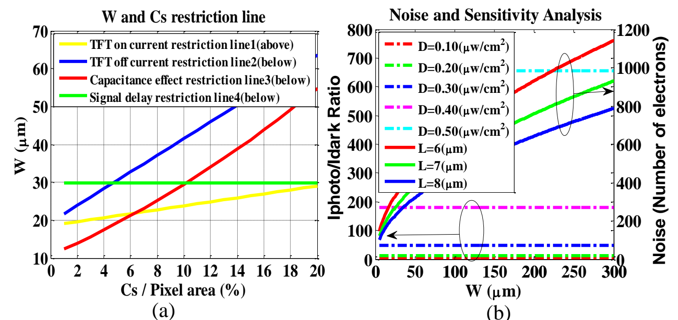


Fig. 1. (a) The analysis of display driving with the channel length(L) of dual-gate TFT is 6 μm; (b) Sensitivity and noise as a function of channel width with various channel lengths and light intensity in a 264 μm×264 μm pixel.

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Surface potential measurement on contact resistance of a-IGZO TFTs by Kelvin probe force microscopy

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***Abstract*—Kelvin probe force microscopy (KPFM) measurement on operating a-IGZO TFT is performed in this work. A clear surface potential drop in the interface between a-IGZO and source/drain electrode is observed, and contact resistance can be extracted directly. This gives a direct evidence for the conclusion that the contact resistance or injection barrier for carriers is controlled by the external biases.**

Keywords*—*Kelvin probe force microscopy (KPFM); a-IGZO; surface potential; Thin Film Transistor

I. Introduction

For a-IGZO TFTs, contact resistance is closely related to the performance of TFTs, however, origin of the contact resistance is still not clear.[1],[2] In this paper, we analyzed contact resistance by using KPFM.

II. Experiment

The heavily p-doped silicon substrate with thermally grown SiO_2 was used as gate electrode and gate dielectric, respectively. The a-IGZO channel layer was deposited by RF magnetron sputtering. Au/Ti stacked layer was deposited as source/drain electrodes by electron-beam vapor deposition and patterned by lift-off process. The surface potential of operating a-IGZO TFT along the channel was measured by KPFM.

III. Results and Discussions

From Figure. 2(a) and 2(b), we can see a sharp surface potential drop at the contact region, and source and drain contact resistances can be obtained from sharp surface potential drop divided by corresponding drain to source current.[3]

In Figure. 3(a), we can see contact resistance is regulated by gate voltage. The reason of gate voltage dependent contact resistance is gate-source voltage and gate-drain voltage can regulate carrier injection barrier at interface of source/drain metal and a-IGZO semiconductor. The carrier injects easier with larger gate-source voltage or gate-drain voltage.

Figure. 3(b) shows drain contact resistance increased with the increased drain voltage, which is equal to gate-drain voltage decreases, and this can attribute to the increased carrier injection barrier at the interface between drain metal and a-IGZO semiconductor. Source contact resistance remained unchanged because of unchanged gate to source voltages.

IV. Conclusions

We obtained contact resistances by KPFM, and we found contact resistances were regulated by gate-source voltage or gate-drain voltage, which attribute to the controlled carrier injection barrier at the interface between source/drain metal with a-IGZO semiconductor

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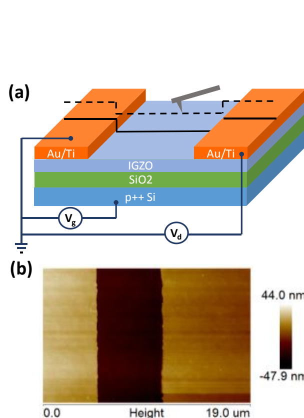

Figure. 1 (a) Schematic diagram of KPFM measuring the a-IGZO TFT. (b) Topography of the fabricated a-IGZO TFT.

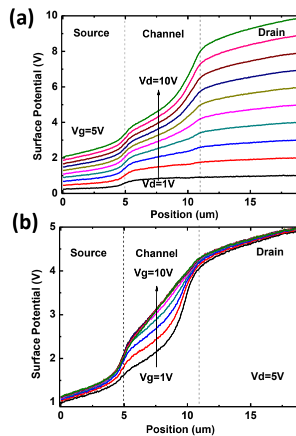

Figure. 2 Surface potential profiles for (a) different drain voltages at constant gate voltage and （b）different gate voltage at constant drain voltage.

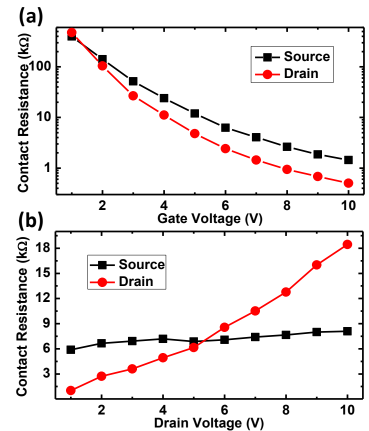

Figure. 3 (a) Source and drain contact resistances as the function of gate voltage and (b) as the function of drain voltage.

Simulation for Unidirectional Ion Flow in TFT-LCDs Induced by AC-Pixel-Driving Signals

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Abstract— Ion flow model for thin-film-transistor liquid crystal displays (TFT-LCDs) is proposed, and a simulation based on this model was conducted to clarify why ions move in one direction with alternating-current pixel-driving signals.

Keywords—TFT ,liquid crystal, ion, multiphysics modelling

I. INTRODUCTION

The mobile markets are demanding TFT-LCDs with excellent image qualities. The fringe field switching (FFS) mode is widely used for these applications. Liquid crystal directors for FFS mode are driven with a lateral electric field, and the electric field intensity near electrodes is much higher than that of the vertical mode. So ions in the liquid crystal cell are easily re-distributed in this strong electric field, and cause image degradations. For example, after displaying white / black (or blue / red) checker patterns for a long time, brighter areas appear on the boundary for a pattern. This boundary image retention occurs because ions move laterally to one side of the displayed pattern. The mechanism for such transport has not been fully analyzed, because the ions were assumed to move only back and forth with alternating current (AC) - electric fields and not in one direction. This paper presents a novel model for explaining why ions move in one direction with AC-pixel-driving signals.

II. MODEL AND SIMULATION

The governing equations for the proposed ion flow model are current, drift-diffusion, and flow equation, as shown in Fig. 1. The time averaged body force <f> is the dielectric force [1] induced on the liquid crystal by the AC-electric field E (ac-E) for the pixel-driving signals. If the high conductivity region (σ1) comes in contact with the low conductivity region (σ2), the transient surface charges of ions (ΔQ) accumulate at their interface when the ac-E is applied.

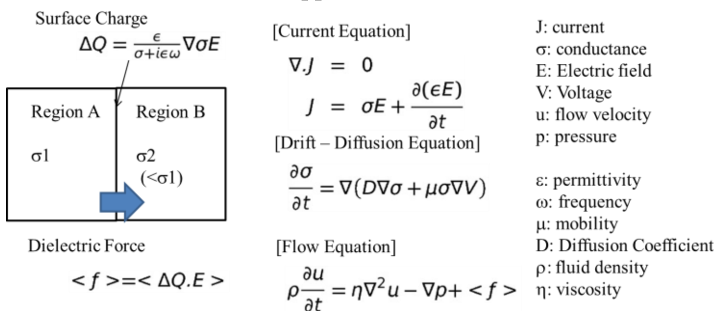

Fig. 1. Governing equations for the proposed model

The ion charging time is slow (1Hz) compared to the pixel-driving signal (30Hz), and the phase of ΔQ is delayed with the ac-E. Thus, the time averaged dielectric force, <f>=<ΔQE>, is not cancelled and exhibits a non-zero value. This non-zero <f> induces the flow in the liquid crystal cell, and the ions move in one direction from the high conductivity region (σ1) to the low conductivity regions (σ2) when the ac-E is applied.

A simulation, incorporating this model, was carried out using the multi-physics FEM solver. Fig.2 shows the geometrical pixel layout for the calculation. The ion profile and net flow around the TFT's contact hole (dotted border area) were simulated. The ion's polarity was set to positive, based on the previous experiment the author conducted. The AC-voltage was applied only to the blue pixel electrodes and not to the red ones. The calculated ion profile and net flow velocity are shown on the right side of Fig. 2. With the capacitive-coupling between the gate and source terminal of the TFTs, the pixel electrode voltage shifted negatively. Therefore, the signal line had a positive offset direct current (DC)-voltage to the pixel voltage. As the positive ions were repulsed with this positive DC-electric field from the signal line, the conductivity around the signal line was lower than those of the other areas. As the AC-pixel driving voltage is only applied to the blue pixel electrodes, the dielectric force was induced only on the blue-pixel region from left (blue-pixel higher conductivity region) to right (signal line lower conductivity region). Thus, the ions flowed from left to right, which is consistent with the boundary image retention phenomenon.

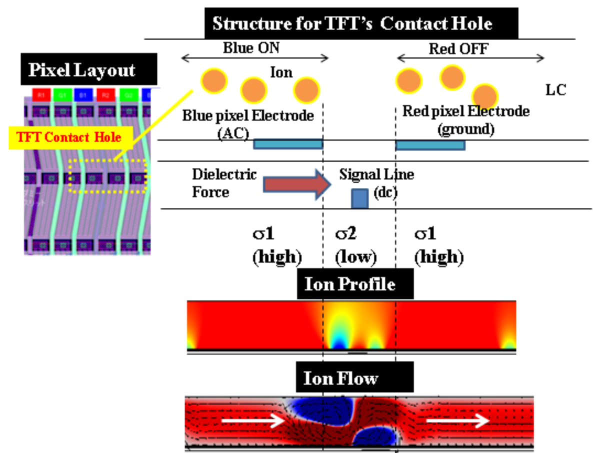

Fig. 2. Geometrical layout, and simulated results for ion profile and ion flow around TFT's contact hole

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Low temperature, stable thin-film transistors based on photopatternable solution-processed InO_x:Li Semiconductors

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***Abstract*—Solution-processed metal oxide (MO) thin-film transistors (TFTs) have attracted great attention for its potential application in flat plane displays (FPDs), electronic papers and sensors, and intensive effects have been devoted to development of MO-TFTs in the field of high mobility, low-temperature process, direct patterning technique and improvement of stability. Herein, we report the fabrication of low-temperature, stable InO_x:Li TFTs based on a green photo-patterning process. The InO_x:Li semiconducting layers, obtained by directly patterning chloride ligand-based indium(III) precursor films using ultraviolet (UV) irradiation and DI water, were integrated on anodized aluminium oxide (AlO_x:Nd) insulators. The InO_x:Li TFTs with 15 at% Li concentration displayed a maximum mobility of 9.6 $cm^2 V^{-1} s^{-1}$ under the annealing temperature as low as 180 ^{o}C and exhibited high stability under both positive and negative voltage bias.**

Keywords*—low temperature; photopatternable; metal oxide; thin-film transistors

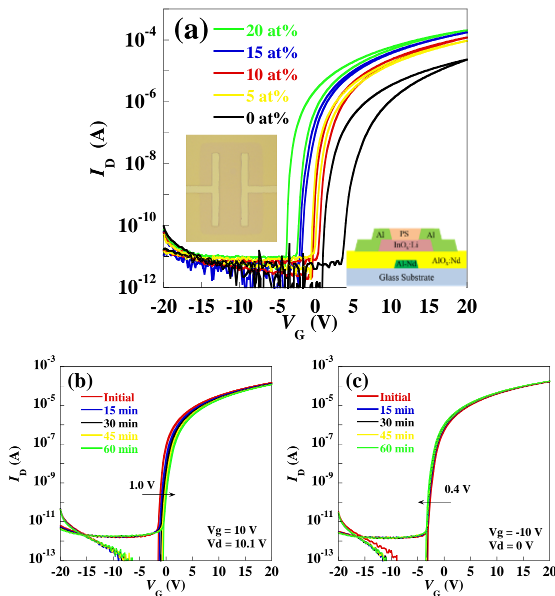

Fig. 1. (a) Transfer characteristics of InO_x:Li TFTs with different Li concentrations; the insect: the microscope image of patterned InO_x:Li TFT. The stability of InO_x:Li TFT with 15 at% Li concentration under (b) positive and (c) negative gate bias.

TABLE I. Summary of mobilities of InO_x:Li TFTs with various concentrations.

Li concentration	0 at%	5 at%	10 at%	15 at%	20 at%
Mobility ($cm^2 V^{-1} s^{-1}$)	1.9±0.5	4.2±1.3	5.3±1.0	8.4±1.3	7.8±0.8

ACKNOWLEDGMENT

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The physical properties of Zn-Sn-N thin films and their TFT application

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***Abstract*—Zn-Sn-N films with nanocrystalline/amorphous mixed phases were fabricated by DC reactive sputtering. The films showed an optical direct bandgap ~ 1.4 eV and an electron mobility ~ 18 $cm^2V^{-1}s^{-1}$. The Zn-Sn-N TFTs with different annealing temperatures were constructed and its electrical properties were analyzed. The Zn-Sn-N channel material shows potential applications in the interactive information display.**

Keywords—interactive display;magnitron sputtering;thin-film transistors; visible light;nanocrystalline

I. INTRODUCTION

Interactive information display (IID) is an important developing trend in the future, which requires the channel material of TFTs to be highly responsive to visible light (E_g < 1.6 eV) [1]. Transparent oxide channel materials (such as InGaZnO, ZnSnO etc.) are intensely investigated due to their sound field-effect mobility, low-cost, low-temperature fabrication, and ease of large-area processability [2]. However, most n-type oxide channel materials have a wide E_g (> 3 eV) [3]. In this work, Zn-Sn-N (ZSN) thin films which have a narrow E_g and acceptable electron mobility were investigated and their TFT application was reported for the first time.

II. EXPERIMENTAL

ZSN thin films and TFTs were fabricated through DC reactive sputtering at room temperature using a Zn/Sn alloy target with the atom ratio of Zn:Sn=6.66:1, at a working power of 120 W and a N_2 working pressure of 2.0 Pa.

III. RESULTS AND DISCUSSION

The XRD pattern shows an amorphous phase of the ZSN film, while the TEM results (Fig. 1a) indicate a nanocrystalline/ amorphous mixed nature. The E_g determined by the α^2 vs. hv curve (Fig. 1b) is 1.44 eV, agreeing very well with the PL result (1.4 eV). The Hall measurement indicates that the film has a $N_e \sim 1.5 \times 10^{19}$ cm^{-3} and $\mu_e \sim 18$ $cm^2V^{-1}s^{-1}$. Fig. 2 shows the transfer characteristics of the ZSN TFTs. The TFT at 250 °C annealing shows a $\mu_{FE} \sim 18.4$ $cm^2V^{-1}s^{-1}$ but a low I_{on}/I_{off} (16), and those annealed at higher temperature shows lower μ_{FE} (1.2 and 0.2 $cm^2V^{-1}s^{-1}$for 300 and 350 °C, respectively) and larger I_{on}/I_{off} (10^7). All in all, the optical and electrical properties of the ZSN films meet the requirement for photo-sensor in IID, however their TFT performance needs further optimization.

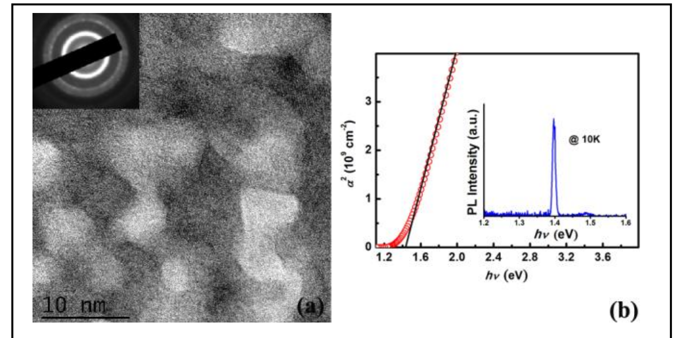

Fig. 1. (a) High resilution transmission electron microscope(HR TEM) image. The inset shows the diffractogram of HR TEM. (b)The α^2 vs. hν curve. The photoluminescence (PL) spuctrum is also shown in the inset.

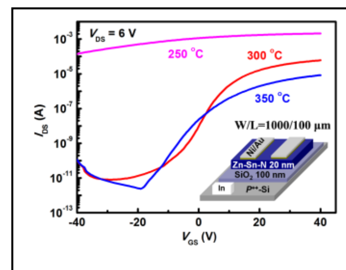

Fig. 2. The transfer curves of the Zn-Sn-N TFTs annealed in N_2 under different temperatures. The inset gives the schematic structure of the TFTs.

ACKNOWLEDGMENT

This work is supported by the Natural Science Foundation of Zhejiang Province (LY16F040002).

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Polymer brush modified surface for high-performance inkjet-printed organic thin-film transistors

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***Abstract*—A morphology control strategy is reported for inkjet-printed small molecular organic semiconductor by using polymer brush. Polystyrene (PS) brushes with different chain length from 4.1 nm to 15.0 nm were grafted onto dielectric by surface-initiated atom transfer radical polymerization (SI-ATRP) and formed uniform and hydrophobic surfaces. The single droplets of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) was inkjet-printed onto PS brushes modified substrates. Self-assembled crystals with large size and highly oriented structure has been exhibited due to long chain length of PS brushes. For the organic thin film transistors (OTFTs) with printed single-dots TIPS-pentacene, the graphene electrodes are used, and the device performance also improved with the increasing chain length of PS brush.**

Keywords—Organic Field-Effect Transistors, Surface Modification.

I. Introduction

Inkjet-printed organic thin-film transistors (OTFT) areattractive electronic devices which has great prospect in flexible display and sensors with superiority of volume controllability and highly spatial selectivity. Since soluble small molecular OSCs have high electric property, these materials have been widely researched. However the strong π-π interactions between organic semiconducting small molecules is likely to induce nonuniform nucleation and film dewetting on substrate. Common SAMs like OTS and HMDS on substrates have low surface energy that cannot effectively pin the three-phase contact line. On another hand, insulating polymer on substrate is also hard to control which may introduce the jaggy interface. Here we present a surface modified method "polymer brush" that incorporates the advantages of SAMs and polymer films, to control the crystalline behaviors of inkjet-printed small molecular OSCs.

II. Experimental Section

Synthesis and immobilization of the silane initiator MTPS-Br, surface-initiated atom transfer radical polymerization, ink-jet Printing and OTFT device fabrication, and characterization.

III. Prepare Your Paper Before Styling

A. *Equations*

Saturated region mobility was calculated by Equation (1):

$$I_{DS} = \frac{W}{2L} C_i \mu (V_{GS} - V_T)^2 \quad (1)$$

B. *Figures and Tables*

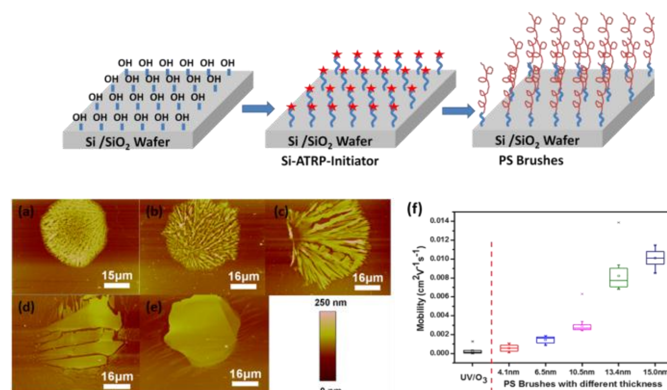

Fig. 1. Synthetic route for PS brush by SI-ATRP method, the AFM measurement images of the drops on the PS brushes with different chain length 4.1, 6.5, 10.5, 13.4, 15.0 nm, and the distribution of mobility on different thickness PS brushes.

Table 1. Electrical properties of OTFTs on different dielectric surfaces.

PS Brushes Length (nm)	Mobility (cm^2 V^{-1} s^{-1})	Threshold voltage (V)	On/Off current ratio
4.1	1.81×10^{-4}	6.67	3.88×10^{3}
6.5	5.31×10^{-4}	3.86	5.04×10^{3}
10.5	7.80×10^{-4}	8.12	5.84×10^{3}
13.4	1.08×10^{-3}	5.60	6.13×10^{3}
15.0	1.93×10^{-3}	4.81	9.07×10^{3}

Acknowledgment

This work was supported by National Natural Science Foundation of China (NSFC Grant No. 51573036 and 21174036)

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O10-02

Low Voltage Organic Thin-film Transistor with Reduced Sub-gap DOS for Power Efficient Logic Circuits

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***Abstract*— Circuit performance of low voltage organic thin-film transistors (OTFTs) using two different approaches including enlarging the gate dielectric capacitance with large permittivity (high-k) gate dielectric material and reducing the sub-gap density-of-states (DOS) at the channel two different approaches were compared by device and circuit hybrid simulations. The simulation results show that low-voltage OTFTs with reduced sub-gap DOS strategy can help to achieve faster and more power efficient circuits.**

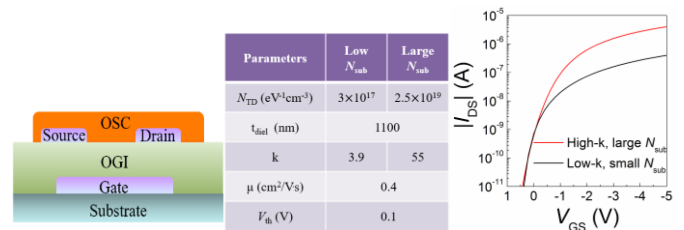
Keywords*— *organic thin-film transistors (OTFTs); low voltage; sub-gap density of states.

I. INTRODUCTION

Reducing the operation voltage is key to enable the organic thin-film transistor (OTFT) technology for many envisioned low voltage and power constrained portable and wearable electronics applications. Two types of approaches have been investigated to realize low voltage OTFTs with relatively thick gate dielectric layer, including enlarging the gate dielectric capacitance with large permittivity (high-k) gate dielectric material [1] and reducing the sub-gap density-of-states (N_{sub}) at the channel [2]. This work compares the circuit performance of a ring oscillator in terms of power consumption (P_{av}), propagation delay (t_p) and power-to-delay product (*PDP*) using the two different low voltage OTFTs by device and circuit hybrid simulations.

II. RESULTS AND DISCUSSIONS

Fig.1(a) and (b) shows the device structure and simulation parameters for two type low voltage OTFTs. The two devices have the same apparent mobility and threshold voltage for device simulations with the commercial tool ATLAS vended by Silvaco. The used semiconductor material models of large and small N_{sub} were extracted from experiments. The gate dielectric constants of two type OTFTs are set to achieve the same SS as shown in Fig.1 (c). The high-k low voltage OTFT presents larger on current compared to the low-k one. The simulated DC and dynamic electrical characteristics of the two low-voltage OTFTs were reproduced by an OTFT compact model in Verilog-A, and incorporated into the HSPICE circuit simulator. The transient performance for the built seven stage ring oscillators based on two different OTFTs were compared based on the key figure of merits, including P_{av}, t_p and *PDP*, as shown Fig. 2. It can be seen that Attributed to the much smaller gate dielectric capacitance, the low-k OTFT circuit presents significantly less power consumption than the high-k one, and can also run much faster although the high-k OTFT has a higher on current. The less power consumption and propagation delay make the low-k OTFT circuit owning a *PDP* value only about tenth of the high-k one.



Parameters	Low N_{sub}	Large N_{sub}
N_{TD} ($eV^{-1}cm^{-3}$)	3×10^{17}	2.5×10^{19}
t_{diel} (nm)	1100	
k	3.9	55
μ (cm^2/Vs)	0.4	
V_{th} (V)	0.1	

(a) (b) (c)

Fig. 1. (a) The device structure and (b) listed parameters for device simulations, and (c) the simulated transfer curves for the OTFTs using different approaches.

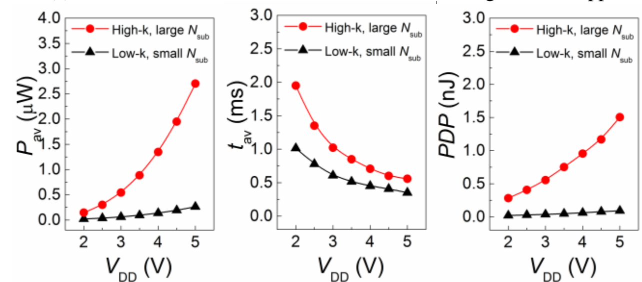


Fig. 2. Extracted P_{av}, t_p and *PDP* for the seven-stage ring oscillators based on two different low-voltage OTFTs.

III. CONCLUSIONS

Comparisons of low-voltage OTFTs based on two different approaches were studied by device and circuit hybrid simulations. The results show that by reducing the sub-gap DOS, OTFT circuit exhibits faster speed and higher power efficiency than conventional low-voltage OTFT by enlarging gate capacitance with high-k dielectric. With material and technology advancements, this device concept would be promising for constructing printable low-voltage power efficient logic circuits.

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A New P-type Shift Register with Detection Function for Flexible Display

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Abstract*—A new p-type shift register for flexible display is proposed in this paper to solve the flexible panel issues. When the panel cannot work well, the P-type shift register can quickly detect which line of circuits has abnormal output, further helping us find out defects of panel. The shift register is not only used to drive the pixel circuits, but also used to detect every line station. Furthermore, the new register consists of only 10 TFTs and 2 capacitors, which helps reduce the layout area and increase the yields of the pan*el. Simulation results show that the p-type shift register can work well.

Keywords—shift register; flexible display; detection

I. INTRODUCTION

It is widely known that the flexible panel display has potential merits such as thinness, lightness, unbreakable, and bendability [1]. A highly flexible panel with good property turns its free shapes a reality, such as rounded, elliptical, and various curved ones [2]. If the flexible panel is curved many times, the panel may not display well and needs some test line points to detect the output of certain line drive circuit. Actually, it is very difficult to detect every row of the drive circuits output. In order to detect it, many test lines are needed, which increase the area of panel and makes narrow border impossible to realize.

II. STRUCTURE DESIGN OF P-TYPE SHIFT REGISTER

In this paper, the scan circuit and EM circuit for driving the panel are proposed. The scan circuit is used to generate low wave pulse with one line. DO/DE (DO is used to detect odd lines output station; DE is used to detect even lines output station) in scan circuit is used to detect every row of low voltage. Odd and even DO/DE lines are separated from each other. Odd-numbered lines are connected together, and even numbered lines are also connected. If they are diverted out, DO/DE can quickly detect it, and DO/DE changes to low voltage, otherwise DO/DE keeps high voltage. If scan shift register has output abnormally, DO/DE will not output low voltage, which helps people quickly find out which line is not working properly and then allows people to fix this line circuit quickly and save the time.

The EM circuit is used to generate high wave pulse with one line. DO in scan circuit is used to detect every row of low voltage. The outstanding advantage is that EM shift register just needs six detect lines DO1~DO6. DO of the first line connects DO of the seventh line and every six lines are connected together, in which DO1 detects 1line, 7line, … , (6n+1)line; DO2 detects 2line, 8line, …, (6n+2)line, and so on. So DO1~DO6 can detect all of EM shift register outputs.

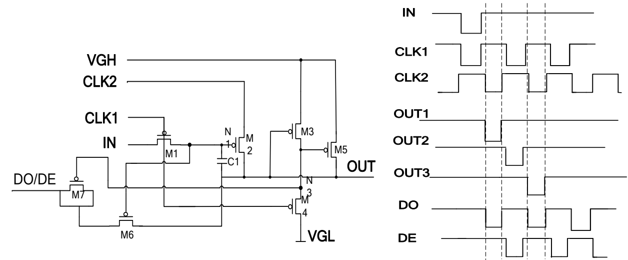

Fig. 1. Scan single stage circuit and timing diagram

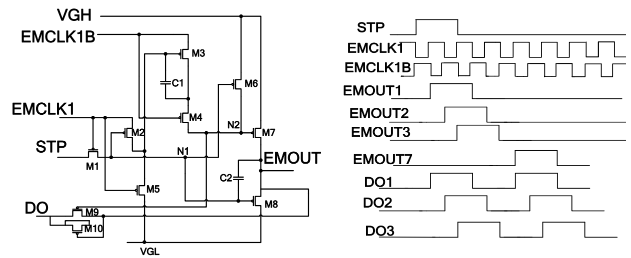

Fig. 2. EM single stage circuit and timing diagram

III. SIMULATION RESULTS AND LAYOUT

The simulation was made by means of the software (Silvaco Gateway), adopting the chosen model (LEVEL-36). The simulation conditions are as follows: the gate line capacitance and resistance are set at 180pF and 10kΩ respectively. It can be shown that DO/DE is capable of detecting output station. From the layout, Scan border length plus EM border length amounts to less than 1000um.

IV. CONCLUSIONS

This paper presents a new P-type shift register with detection function for flexible display. The shift register can be not only used to drive pixel, but can also detect the line of pixel work station without influencing the border of panel, making it suitable for flexible panel to quickly detect panel work station.

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Computable Flexible Electronics: Circuits Exploring for Image Filtering Accelerator with OTFT

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***Abstract*—Flexible electronic devices are widely adopted in fields of sensors, wearable equipments, RFID and large-area applications, for their features of bending and stretching. However, relatively fewer research works on computation with flexible electronic devices are reported, due to their poor carrier mobility and stability. In this paper, a novel circuit architecture of image filtering accelerator using Organic Thin-film transistor (OTFT), which could realize real-time image signal convolution in analog domain, is proposed.**

Keywords—Flexible electronics; OTFT; Image processing; Gaussian convolution; Physical computing

I. Introduction

With rapid improvement of manufacturing technology, flexible electronics has achieved great progress and received much attention. However, despite benefits of low-cost and ease of fabrication, intrinsically low carrier mobility and large parameter variability has become an obstacle to its wider applications. This paper presents a real-time and energy-efficient implementation of image Gaussian convolution accelerator based on analog Gilbert multiplier [1] and OTFT technology, which overcomes disadvantages of flexible devices.

II. Circuits and Architecture

As illustrated in Figure 1, the overall system architecture employs the concept of physical computing, where computing could be done right after sensors obtain the original analog data. This architecture is aimed to realize a whole flexible system including sensor, memory, data converter and signal processing. The image sensor is supposed to be active pixel sensor (APS) and outputs of pixels are directly attached to inputs of the Gaussian convolution unit. Input voltages are generated from on-chip memory and DACs thus the filter is programmable. Convolution output could be buffered and read out by ADC in serial, under the control of address and bus controller. Without clock participation in convolution progress, calculating time is only related to settling time of the circuit. So with the idea of physical computing, the image filtering could be implemented in real time with relatively slow OTFTs.

The core computing circuit is Gilbert Gaussian multiplier [1] (Shown in Figure 2(a)). By adjusting input voltages could achieve multiplications of input currents and weights; and addition could be realized by attaching the multipliers' outputs together due to current-mode output.

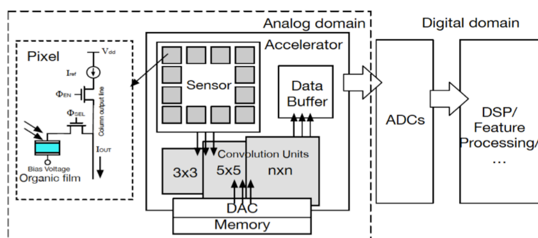

Fig. 1. System Architecture.

III. Simulation and Analysis

A 128×128 test image is used as simulated sensor output and circuit simulation is done by Cadence with OTFTs modeled by a level-62 spice model. The images after Gaussian filtering are shown in Figure 2(b). The PSNR of two scales is 54.1dB and 50.7dB respectively. The settling time of Gaussian convolution circuit is about 300ns, equivalent to perform convolution operation at a frequency of 3.3MOP/s. The power consumption is related to the scale of Gaussian convolution unit. We take VGA-format (640 × 480) images as example. Given convolution kernel is 5×5 in size, every Gaussian unit contains 25 multipliers, which consumes $25\times1.8v\times1\mu A = 45\mu W$ in total. In order to realize real-time processing, at least 3 units should work in parallel. Thus the total power consumption is $3\times45\mu W = 135\mu W$ and the time is $640\times480 \div 3.3MOP/s \div 3 = 0.031s$, that is 32 fps in image processing.

TABLE I. Simulation Results

Settling time of Gaussian convolution unit	Convolution operation frequency	Power consumption of real-time processing VGA images	PSNR of Lena image
300ns	3.3 MOP/s	135μW	54.1dB (σ = 1.5450); 50.7dB (σ = 1.9466)

IV. Conclusion

In this paper, a novel design method is proposed to make it possible for flexible TFTs to implement real-time and energy-efficient computation. Our work has made endeavors towards **computable flexible electronics for full system**, which would be parts of sensors, amplifiers, and data converters, as well as computing modules for complex algorithms [2].

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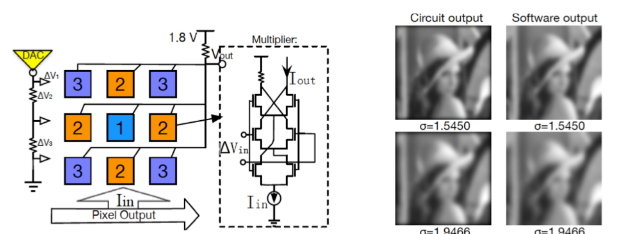

(a) Gaussian convolution unit. (b) Comparison of circuit and software output.

Fig. 2. Gaussian concolution unit & comparison of outputs.

Heart Rate/Impulse Monitoring Using Autonomous PVDF-Integrated Dual-Gate Thin-Film Transistor

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***Abstract*—In wearable electronics, autonomous sensor can potentially ease the usage of bulky battery and eventually lead to a sustainable system. In this paper, polyvinylidene fluoride (PVDF) piezoelectric film-integrated dual-gate thin-film transistor (TFT) is utilized to monitor human vital signs such as heart rate or impulse rate. The voltage generated by the PVDF from the impulse itself drives the TFT that rectifies and converts impulse signal to the weak current signal feeding to the low-noise amplifier. The preliminary results of such device in addition to system design of chip-based sensor-integrated RFID tag are addressed to unveil the promising applications in wearable electronics.**

***Keywords*—Dual-gate TFT, radio frequency identification (RFID), autonomous sensor, heart rate monitoring.**

I. Introduction

In terms of reducing power consumption, low-power chips and microprocessors have greatly advanced the state of the art in wearable electronics [1]. Thanks to the rapid development of smart integrated sensor and efficient data processing, the RFID tag integrated with sensors that monitor physiological parameters (temperature, heart rate, respiration rate and etc.) can be achieved [2]. However, the major hindrances remain in using external power sources such as battery to drive various analog sensors. We proposed a device concept of energy harvester using PVDF-integrated dual-gate TFT to power wearable sensors. In this paper, we will implement the same device concept to realize an autonomous sensor for heart rate and impulse monitoring.

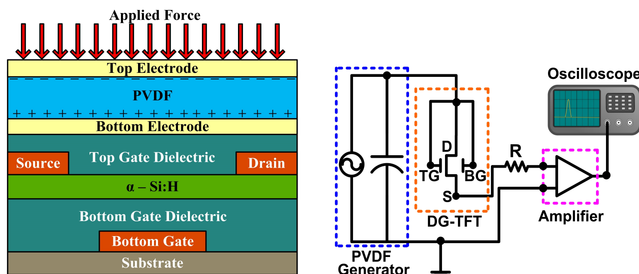

Figure 1: (a) Device structure and (b) Equivalent circuit.

II. Device Architecture

The proposed device is essentially a piezoelectric polyvinylidene fluoride (PVDF) based power generator in conjunction with a dual-gate thin-film transistor (DG-TFT) that has four terminals i.e., a top gate (TG) that is merged with the bottom electrode of PVDF, a bottom gate (BG), a source terminal (S), and a drain terminal (D) as seen in Fig. 1(a). In an autonomous mode, TG, BG, and D are connected while S is connected with a resistor as shown in Fig. 1(b). The voltage generated by the PVDF modulates the channel resistance of the TFT and biases the channel and eventually leads to the current change. Additionally, there is no need for the external rectifier as the DG-TFT serves for the purpose of rectification as well during its operation. Thus, the generated signal is weak enough and needs to be amplified for application purposes.

III. Heart Rate/Impulse Monitoring

The rectified output from DG-TFT is then fed to high impedance signal amplifier for heart-rate or arterial impulse monitoring. The preliminary results of the PVDF-integrated DG-TFT in conjunction with a low-noise amplifier in the event of heart rate monitoring was presented in Fig. 2. Moreover, a system level approach of an autonomous sensor integrated with active RFID tag is shown in Fig. 3.

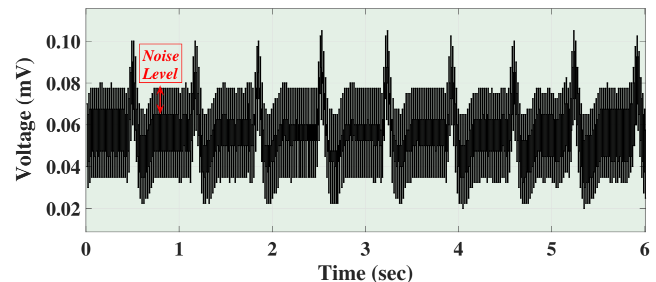

Figure 2: Preliminary experimental results on heart rate/impulse monitoring.

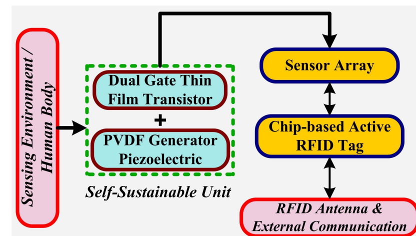

Figure 3: System level approach for sensor integrated RFID tag.

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Failure mechanism of TFT devices on flexible substrate by cyclic bending test

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Abstract — **In this paper, the failure mechanism of TFT devices on flexible substrate was investigated using bending test. The results show that the TFT fails due to the micro-cracks in M_2 lines; the micro-cracks first generate at the brittle layers and then migrate to the M_2 lines.**

Keywords — TFT; failure mechanism; cyclic bending test

Introduction

Active-matrix organic light-emitting diode (AMOLED) has been widely used in flat panel displays due to its wide viewing angle, light weight, vivid color. The flexible displays become possible as the AMOLED can be prepared on flexible substrate. When the flexible display is bent, twisted or stretched, the device experiences certain strain and the layer in TFT will rupture and the electrical properties will fail when the strain exceeds their critical strain. The bending properties of TFT have been widely studied; however, the failure mechanism has not been deeply understood [1]. In this work, the failure mechanism of LTPS (Low Temperature Poly-silicon) TFT devices on flexible substrate was investigated using cyclic bending test. The micro-cracks generated in brittle layers migrate to the source and drain metal (M_2) lines and then the electrical properties of the TFT device fail.

Experiment

First, the LTPS TFT was prepared on PI substrate. Second, SiN_x/SiO_x multilayer was deposited by CVD as barrier layer. Then the p-Si channel, GI (SiO_x) and passivation layer (SiN_x) were respectively deposited by CVD. At last, the photoresist was then spin coated as planarization layer. The gate Mo and source/drain Mo/Al/Mo electrodes were prepared by magnetron sputtering method. The TFT device was face-out bending for 100 000 cycles when the bending radius (R) is 3 mm.

Result and discussion

The thickness of the substrate and the TFT device are 12 µm and 4 µm, respectively. The surface tensile strain of the TFT film bent to a radius of curvature R is: $\varepsilon = (d_{PI}+d_{TFT})(2\eta\chi+1)/2R(\eta\chi+1)$, where $\chi = E_{TFT}/E_{PI} = 200$ GPa/7.9 GPa ≈ 25.3, and $\eta = d_{TFT}/d_{PI} = 4$ µm/12 µm ≈ 0.3 [2]. The ε in TFT is about 0.5%. Fig. 1(a) shows the I_d-V_g curves of the LTPS before and after bending test. The results show that the sample completely fails after 100 000 cycles. The Fig 1b and Fig 1c are the optical and SEM pictures of the TFT device after bending test, respectively. Fig 1c is larger version of Fig 1b. Rig. 1 and Rig. 2 are two vital parts in TFT device: metal line and TFT itself. From Fig 1b, micro-cracks generate in metal line (Rig. 1) while no crack is found at the same region from SEM pictures. As the SEM picture can only reflect the surface morphology of the sample, we infer from this interesting thing that the micro-crack generate not in the surface but in the inner structure of the TFT device. In order to get more details, the cross-section of the TFT region and the M_2 region are studied by Focused Ion Beam (FIB). No crack appear along the TFT region, indicating that no mechanical failure happen in the key layers (channel, GI, passivation layer, planarization layer) in TFT. From the cross-section of metal line, micro-cracks generate at the SiN_x/SiO_x barrier layers and then propgate to the M_2 layer, after that micro-cracks extend to the passivation layer and stop at the planarization layer. The FIB results shows that the failure mechanism of the TFT device is not the TFT itself but the rupture of the M_2 lines. The brittle layer ruptures, causing the micro-crack to propagate to the M_2 line and then the TFT devices lose its electrical properties.

Conclusion

In conclusion, the fracture mechanism of the TFT device is investigated by bending test. The TFT device fails after bending test. The failure mechanism of the TFT device is not in TFT itself but the rupture of the M_2 lines. The micro-crack occor at the brittle SiN_x/SiO_x layers and then migrate to the M_2 lines, the rupture of M_2 line leads to the failure of the TFT devices. More work is needed to improve the reliability of the M_2 line to improve the mechanical reliability of the TFT devices.

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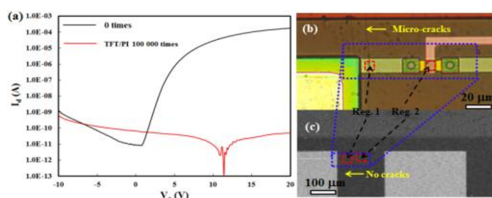

Fig. 1. (a) I_d-V_g curve, (b) optical image and, (c) SEM image of LTPS.

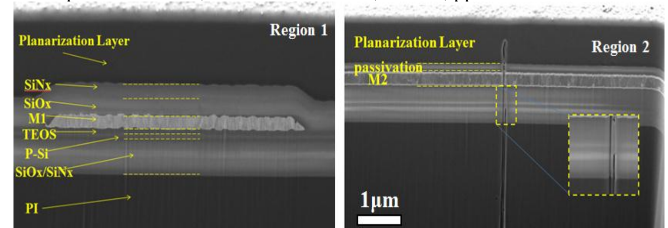

Fig. 2. SEM images of region 1 and region 2.

Bendable Corbino a-IGZO TFTs

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***Abstract*— In this work, stability of flexible amorphous-indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs) with a Corbino (circular) structure is investigated under extreme bending conditions and The TFTs are found to exhibit excellent stability when bent to a radius of 0.5 mm (which corresponds to a tensile strain of 1.7%) for 10000 cycles. Good stability of the Corbino TFTs is attributed to a uniform electric filed distribution, owing to the circular structure, and the ability of the large outer-ring electrode to deplete electrons in the channel. Corbino a-IGZO TFTs could, therefore, be useful in next generation bendable display backplanes, given that they also exhibit infinite output resistance beyond pinch-off.**

Keywords*— *Circular, corbino, TFT, IGZO, flexible

I. Introduction

Mechanical bending stability of flexible displays is determined mainly by the bending stability of the thin-film transistor backplane. It is, therefore, necessary to develop a TFT that is very stable under mechanical bending stain for the future of flexible displays. In this study, the stability of amorphous-indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs) with a Corbino (circular) structure is investigated.

II. Result and Discussion

The Corbino structure is composed of inner and outer concentric ring electrodes Fig. 1, which are the equivalents of a source and drain in rectangular TFTs. The Corbino TFTs are measured in the flat state and then while bending to a radius of 0.5 mm, which corresponds to a tensile strain of 1.7%. It can be seen in Fig. 2 that the Corbino TFTs exhibit excellent stability, even when the mechanical bending strain is applied for up to 10000 cycles. Note the Corbino TFTs exhibit infinite output resistance beyond pinch-off, as previously reported [1]. The good stability exhibited by the Corbino TFTs is attributed to a more uniform electric field distribution across the circular channel and a lesser total channel charge concentration in Corbino TFTs, owing to the larger outer-ring electrode, which depletes more electrons than the drain of rectangular TFTs [2].

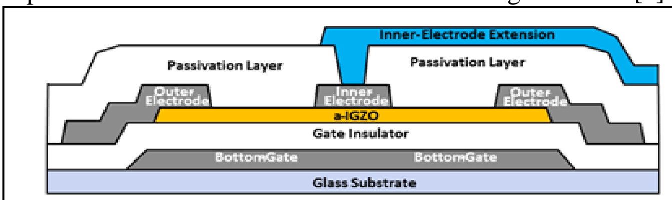

Fig. 1. (a) Schematic cross section of Corbino a-IGZO TFT

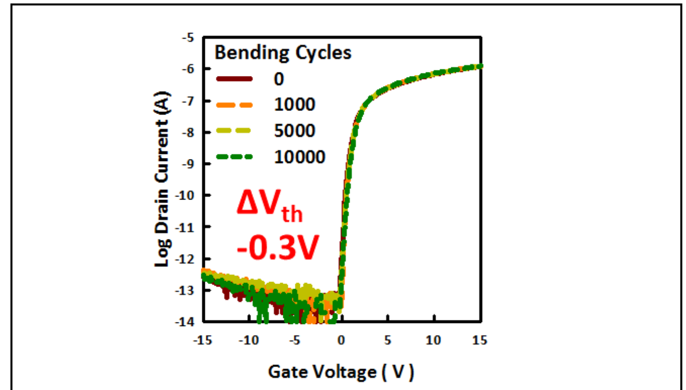

Fig. 2. Bending stability of Corbino a-IGZO TFT transfer.

III. Conclusion

The flexible Corbino a-IGZO TFT is proposed as a solution for mechanical stability. Under 1.7% strain Corbino exhibit excellent performance, and thus can be applied to flexible display backplane technologies.

Acknowledgment

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High-mobility flexible thin-film transistors with zirconium-doped indium oxide channel layer

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***Abstract*—A novel ZrInO semiconductor material was investigated as an active channel material for the oxide TFTs. The flexible ZrInO TFT exhibited excellent electrical characteristics with a saturation mobility (μ_{sat}) of 22.6 cm^2 V^{-1} s^{-1}, an on/off current ratio (I_{on}/I_{off}) of 2.51 × 10^7, a subthreshold swing (SS) of 0.39 V/decade, a positive ΔV_{th} of 1.89 V under PBS and a negative ΔV_{th} of −1.56 V under NBS. In addition, the flexible ZrInO TFT was able to maintain the relatively stable performance at bending curvatures larger than 20 mm.**

Keywords*—flexible; ZrInO; thin film transistors; low temperature;

I. INTRODUCTION

Recently, great attention has been focused on the flexible active matrix organic light-emitting diodes (AMOLEDs) because of its superior properties such as lightweight, flexibility, bendable, unbreakable and wearable [1-3]. Flexible thin film transistors (TFTs) as the key part have attracted increasing attention and there are some reports on the flexible TFTs. But the mobility for most of these flexible devices are about 5–15 cm^2 V^{-1} s^{-1} which is not enough for future flexible high-resolution, high-frame rate, or 3D displays. Therefore, the higher bending properties and higher mobility is still the main objective for the next flexible oxide TFTs.

In this paper, a novel ZrInO semiconductor material was investigated as an active channel material for the oxide TFTs. Fig. 1 shows the bending flexibility of the ZrInO TFT under different bending curvatures of 30 mm, 20 mm and 10 mm. And the detailed properties were summarized in Table I, the flexible ZrInO TFT exhibited excellent electrical characteristics with a saturation mobility (μ_{sat}) of 22.6 cm^2 V^{-1} s^{-1}, an on/off current ratio (I_{on}/I_{off}) of 2.51 × 10^7, a subthreshold swing (SS) of 0.39 V/decade, a positive ΔV_{th} of 1.89 V under PBS and a negative ΔV_{th} of −1.56 V under NBS. In addition, the flexible ZrInO TFT was able to maintain the relatively stable performance at bending curvatures larger than 20 mm.

II. ACKNOWLEDGMENT

The authors are grateful to the National "863" Project of China (Grant no. 2014AA033002), the National "973" Project of China (Grant no. 2015CB655000), the National Natural Science Foundation of China (Grant nos. 61204087, and 51173049).

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TABLE I. SUMMARY OF THE CHARACTERISTICS OF THE ZRINO FLEXIBLE TFTS BEFORE AND AFTER BENDING.

Radius of curvature (mm)	V_{on} (V)	$I_{on/off}$	SS (V/decade)	μ (cm^{2}V^{-1}s^{-1})	ΔV_{th} (V)	
					PBS	*NBS*
initial	3.56	2.51 × 10^7	0.39	22.6	1.89	1.56
30	3.56	2.51 × 10^7	0.40	22.8	---	---
20	3.56	2.51 × 10^7	0.41	22.6	---	---
10	3.56	6.33 × 10^4	0.76	21.8	---	---

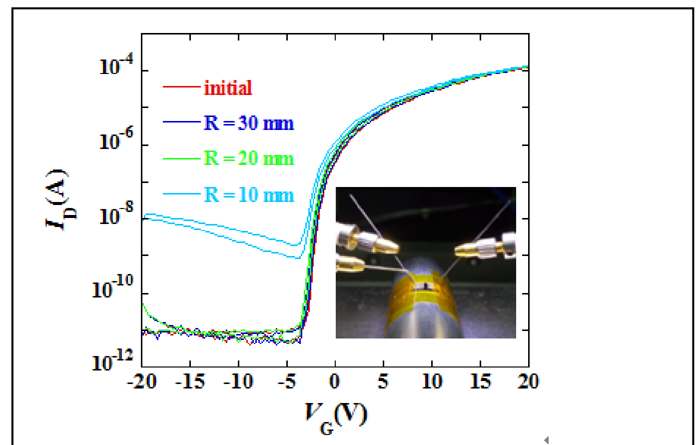

Fig. 1. Transfer characteristics of flexible ZrInO TFT under bending conditions. Inset: the image of equipment in bending test

Organic-inorganic Hybrid Ambipolar Field-effect Transistor with a Cytop interlayer

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***Abstract*—Ambipolar field-effect transistors (FETs) have received significant attention due to their potential applications in complementary logic circuits, which can overcome the limitations of integrated circuits that use only unipolar logic. Organics and metal oxide semiconductors are two families of materials that are currently being investigated as potential alternatives to silicon (Si) technology for use in existing and new electronic device applications. In the case of OFETS, low mobility and reliability are major difficulties. On the other hand, inorganic metal oxide semiconductors are inexpensive and solution processable. Many oxide semiconductors show significantly high electron mobility, although p-type materials show very poor hole mobility. Ambipolar FETs were successfully fabricated composed of an upper pentacene layer and a lower sulotion-proecessed InO_x layer. With Cytop inserted into the interface, the ambipolar FETs exhibit good performance with hole and electron mobilities of 0.12 and 0.26 cm^2 V^{-1} s^{-1}, respectively. We combine the organic ambipolar transistors into functional CMOS-like inverters.**

Keywords—field-effect transistors; organic-inorganic; ambipolar; Cytop; inverter

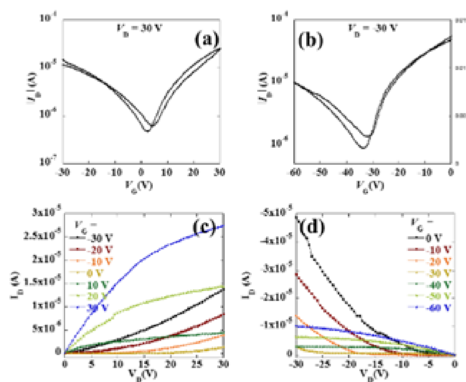

Fig. 1. Transfer and output characteristics of ambipolar FETs.

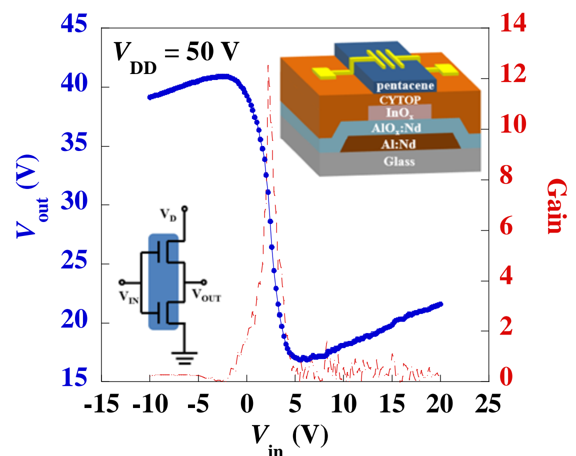

Fig. 2. Voltage transfer characteristics and voltage gain ($|dV_{out}/V_{in}|$) of an complementary-like inverter.

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Contact Length Optimization in Organic Thin-Film Transistors

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***Abstract*— The contact resistance and cutoff frequency in staggered organic thin-film transistors (OTFTs) with different contact length was studied. The effect of gate–source voltage, channel length, semiconductor film thickness, mobility, material disorder, anisotropy of mobility, and Schottky barrier between organic semiconductor and source/drain electrodes were considered. The simulation results show that the contact resistance did not increase obviously until the contact length was scaled down to sub 500 nm and the highest cutoff frequency could be obtained with contact length in the range of sub 100 nm with Ohmic contacts.**

Keywords—Organic thin film transistor (OTFT), contact resistance, cutoff frequency, contact length.

I. Introductionn

As one of the potential candidates of applications in displays, sensors, and RF identification tags, organic thin-film transistors (OTFTs) have attracted significant attention due to its low price and excellent flexibility [1], [2]. Many valuable studies were implemented on optimizing overlap length [3-6]. However, only limited efforts was put into the field of device architecture such as channel length, mobility, material disorder, anisotropy of mobility systematically. Based on the solution of Poisson-Boltzmann equation in staggered OTFTs, L_c downscaling potential was systematically performed.

II. Model Theory And Results

The device structure discussed in this letter is illustrated in Fig. 1a. In our simulation, gate electrode overlaps the entire source/drain contacts. The channel current (I_{ds}) will start to spread into drain contact nears the edge of electrode (at the position of V_0 as is shown in Fig. 1b, I_{ds} will spread). As illustrated in Fig. 1c, most of I_{ds} flows into drain contact in a narrow range near channel, indicating that L_c has great potential for down scaling. The parameters used here are W = 500 µm, $\varepsilon_r = 3$, $C_{ox} = 5.3 \times 10^{-8}$ F/cm^2, $n_i = 5 \times 10^{14}$/cm3, T = 300 K, $V_{ds} = 1$ V, and the thickness of insulator layer is 50 nm.

Based on the solution of Poisson-Boltzmann equation, The simulation results show that the contact resistance did not increase obviously until the contact length was scaled down to sub 500 nm and the highest cutoff frequency could be obtained with contact length in the range of sub 100 nm with Ohmic contacts. The results will provide significant guidelines for improving frequency and saving electrodes materials of printable OTFTs.

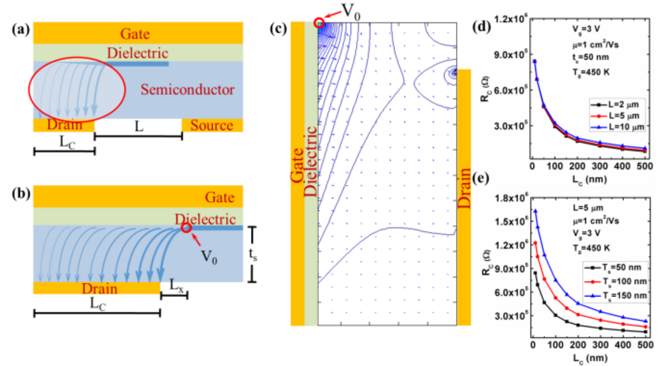

Fig. 1. (a) Schematic cross section of top gate staggered OTFT. Lc is the contact length. (b) Schematic of OTFT at drain electrode side. V0 is the voltage at the position that channel current (Ids) start to spread into drain electrode, Lx is the distance between spreading point and the drain electrode edge, and ts is semiconductor film thickness. (c) Schematic of current distribution at drain electrode side, most of Ids flows into drain in a narrow range near channel. Simulation of the relationship between total contact resistance and contact length with different (d) Channel length,(e) Semiconductor film thickness.

Acknowledgment

This work was supported by the National Natural Science Foundation of China (No. 61574107, 51503167), and Fundamental Research Funds for the Central Universities (JB151402).

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Charge trapping performance based in $Zr_{0.5}Hf_{0.5}O_2$ for nonvolatile memory

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***Abstract*—In this study, the charge trapping memory device based on $Zr_{0.5}Hf_{0.5}O_2/SiO_2/Si$ simple structure was investigated. The memory device annealing at 690°C shows a good behavior with a memory window of 5.6 V under ±12V sweeping voltages in its capacitance-voltage curve and a stable retention property.**

***Keywords*—$Zr_{0.5}Hf_{0.5}O_2$; annealing; charge trapping memory;**

I. Introduction

Nonvolatile flash memories have been widely applied.[1] Among the nonvolatile flash memories, the charge trapping memory (CTM) device, such as silicon-oxide–nitride-oxide–silicon (SONOS) memory devices, attract much attention due to the wonderful endurance and retention property over the floating-gate device, fast program/erase speed, and the compatibility with high-density scaled CMOS technology.[2] In this letter, we designed the $Au/Zr_{0.5}Hf_{0.5}O_2/SiO_2/Si$ structure by a simple fabrication procedure, in which the $Zr_{0.5}Hf_{0.5}O_2$ films work as charge trapping layer and blocking layer.

II. Experiment

P-type Si wafer with a resistivity of 1-10 Ω cm were cleaned by the standard Radio Corporation of America (RCA) process. Then the 50 nm $Zr_{0.5}Hf_{0.5}O_2$ films were deposited by RF-magnetron sputtering technique with base and working pressures of 2×10^{-4} Pa and 3 Pa. After deposition, the sample was undertaken a RTA at 690 °C in O_2 atmosphere for 5 minutes, which is in order to generate the tunnel SiO_2 layer. Finally, Au top electrodes with an area of 7.85×10^{-5} cm^2 were fabricated by vacuum evaporation technique.

III. Results And Discussion

As shown Fig 1, the memory window of the sample with RTA temperature of sample was about 5.6 V, when the applied voltage is 12 V. This result indicates that the magnetic sputtering deposited and annealing process disposed $Zr_{0.5}Hf_{0.5}O_2$ film can provide a high density of charge traps. Fig 2, we discover the retention property is good, indicating the inter-diffusion layer and the SiO_2 tunneling layer having an important role for the retention property of the capacitors. Form the fig 3, we can easily find that the thickness of SiO_2 layer between the $Zr_{0.5}Hf_{0.5}O_2$ and Si substrate is 2.5 nm.

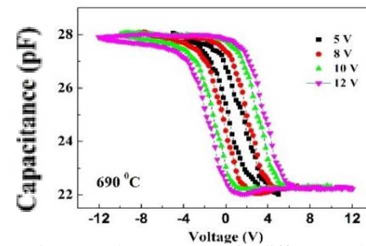

Fig. 1. The C-V curve in different voltages.

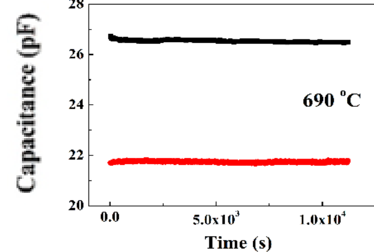

Fig. 2. The retention of the capatitance.

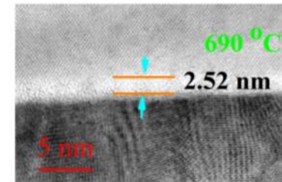

Fig. 3. The TEM image of simple.

IV. Summary

We fabricated CTM devices with $Zr_{0.5}Hf_{0.5}O_2$ grown on Si substrate and annealed it at 690°C though PDA process. The charge trapping characteristic has a large memory windows, reasonable retention and trap density.

Acknowledgment

This work was financially supported by Natural Science Foundation of China under a grant No. of 61306098

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A Physical Model for Double Gate Amorphous InGaZnO Thin Film Transistors Based on Multiple Trapping and Release Mechanism

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***Abstract*—In this work, a physical model for double gate (DG)amorphous InGaZnO (a-IGZO) thin film transistors (TFTs) was proposed based on multiple trapping and release mechanism. Calculation results of I-V characteristic based on this model agree well with the experimental data. The observed mobility's transition to "band like" transport at different top gate bias in DG a-IGZO TFTs can be recovered. The inner physical properties of DG a-IGZO TFTs, such as electric potential and carrier concentration, were also analyzed based on the proposed model. It turns out that bulk accumulation of transport carrier occurs at high top gate bias in DG configuration.**

Keywords—a-IGZO TFTs, dual gate, physical model, multiple trapping and release mechanism.

I. INTRODUCTION

Amorphous oxide semiconductors, for example amorphous InGaZnO (a-IGZO), based thin film transistors (TFTs) are of increasing interest for potential flexible, transparent, and large area fabrication friendly applications. However, the charge transport for a-IGZO remains unclear. In this work, based on multiple trapping and release mechanism, we proposed a physical model for DG a-IGZO TFTs. We also analyzed some inner physical properties, such as electric potential and carrier concentration, of the DG a-IGZO TFTs.

II. EXPERIMENT

A DG a-IGZO TFT was fabricated with the structure with the a-IGZO layer of 20nm. 60nm thickness and 120nm molybdenum (Mo) were used as bottom and top gate electrode, respectively. A bilayer of SiN_x (100nm) and SiO_2 (150nm) was deposited as bottom dielectric layer, a 300nm thick SiO_2 was deposited as the top dielectric layer, and a Mo layer was used as source and drain electrodes.

III. RESULTS AND DISCUSSIONS

Fig. 1a shows the comparison between experimental data of the transfer characteristic by sweeping bottom gate voltage with different constant top gate voltages and fitting results by our model. The fitting results in Fig. 1a shows that the model can well describe the top gate's modulation to the threshold voltage of a-IGZO TFTs. In Fig. 1b, one can see that, with the same parameters, we can fit the output characteristic well.

One interesting result of our previous publication is that band-like transport (field-effect mobility decrease with the increase of temperature) occurs when top gate voltage biased at negative voltage, while activated transport maintains at positive top gate voltage. The calculation results capture these experimental data well, as shown in Fig. 1c. Fig. 1d shows the calculation result of the comparison of asymmetric operation and symmetric operation of a-IGZO TFTs.

IV. CONCLUSIONS

Multiple trapping and release mechanism was included in the proposed physical model for DG a-IGZO TFTs. The proposed model can fit well with experimental data. Using the model, performance of DG a-IGZO TFTs with different structures and operation modes can be predicted.

V. ACKNOWLEDGMENTS

This work was supported by the Strategic Priority Research Program through the Chinese Academy of Sciences under Grant XDB12030400.

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Figures:

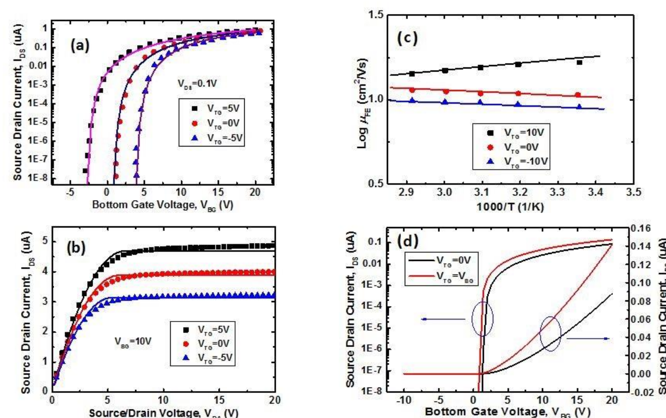

Figure. 1 (a) Transfer characteristic of a-IGZO TFTs. (b) output characteristic of a-IGZO TFTs. (a) Temperature dependent field-effect mobility of dual gate a-IGZO TFTs at different top gate voltage. (b) Comparison between the calculation results by the model between asymmetric operation and symmetric operation of a-IGZO TFTs.

Three-Dimensional Fin-Shaped Dual-Gate Photosenstive a-Si:H Thin-Film Transistor for Low Dose X-Ray Imaging

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***Abstract*—This work reports on a novel dual-gate photosensitive amorphous silicon (a-Si:H) thin-film transistor (TFT) for low-level light detection. To enhance carrier collection and light absorption while maintaining decent switching performance, a three-dimensional (3D) fin-shaped channel is designed and verified. As a result of field strengthening particularly nearby the contact regions, the sensitivity parameter γ_{Dark}=–0.84 is obtained. Hence, the device tends to have a wider dynamic range compared with the previous Pi-shaped and planar structures [1, 2]. The TFT is very sensitive to the light of 550 nm and the photoconductive gain exceeds 100, making it a sound promise for low-dose indirect-conversion X-ray imaging.**

Keywords—fin-shaped channel; dual-gate photosenstive TFT; amouphous silicon (a-Si); low-dose X-ray imaing;

I. Introduction

X-ray imaging is widely practiced in medical diagnostics. Conventional flat panel X-ray detector is composed of a sensor, a capacitor and a switch, all the three components are fabricated separately, which will result in design complexity and low resolution. Our group proposed a-Si:H dual-gate photosensitive TFTs that combine the above mentioned three components [1, 2]. In order to further improve the photo sensitivity and dynamic range of the dual-gate photosensitive TFTs, hereby we report on a 3D fin-shaped structure and conduct the preliminary study on this device.

II. Device Structure and Electric Field Simulation

Fig. 1 provides a cross-sectional view of a fabricated fin-shaped dual-gate TFT by FIB-SEM. The fabrication is a six-mask process, which is compatible with conventional TFT-LCD technologies.

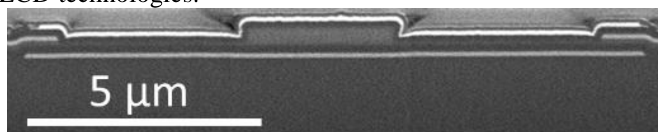

Fig. 1. Scanning Electron Microscopy (SEM) cross-sectional view of a fabricated fin-shaped dual-gate a-Si:H TFT.

COMSOL simulation shows that the electric field is strengthened in the source/drain regions and accordingly the charge collection efficiency will be enhanced.

III. Results and Discussion

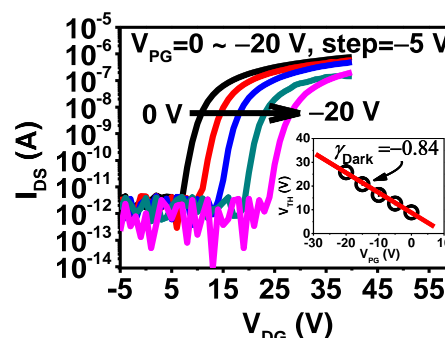

Fig. 2. Transfer characteristics of a fin-shaped dual-gate a-Si:H TFT under different top gate bias. V_{DS}=1 V.

The sensitivity parameter γ_{Dark}, an indicator of the threshold voltages dependence on the top gate voltages, is –0.84, which is higher than the value in our previous reports [1, 2]. Thus, the threshold voltage can be tuned in a wide range to improve the dynamic range. The TFT responds quickly and intensively upon 550 nm-pulse green light exposure and the photoconductive gain is higher than 100 due to the amplification of the bottom TFT. The wide dynamic range and high sensitivity make the 3D fin-shaped TFTs promising for low-dose indirect-conversion X-ray imaging.

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Subthreshold Operation of PVDF-Integrated Dual-Gate Thin-Film Transistor for Tactice Sensing

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***Abstract*—This paper presents a piezoelectric-charge-gated thin-film transistor (TFT) operated in the subthreshold region intended for tactile sensing. The TCAD simulation has been conducted to detail the working principles of the device in the subthreshold region together with experimental results on a fully-integrated sensor using polyvinylidene difluoride (PVDF) and a-Si:H dual-gate TFT.**

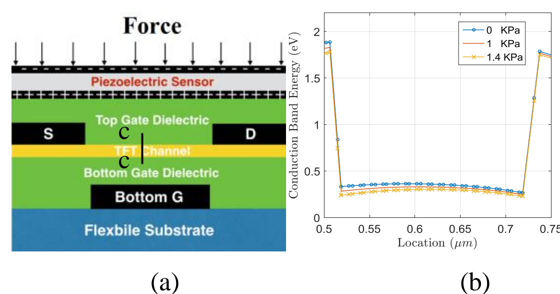
Keywords*—*PVDF; dual-gate thin-film transisitor; TCAD simulation; subthreshold operation; tactile sensing.

I. Introduction

Thin-film transistor has been widely used in active matrix liquid crystal displays and organic light emitting diode displays. We proposed a tactile sensor using piezoelectric-charge-gated TFT where a discrete PVDF film was connected with a top gate of a TFT structure [1, 2].

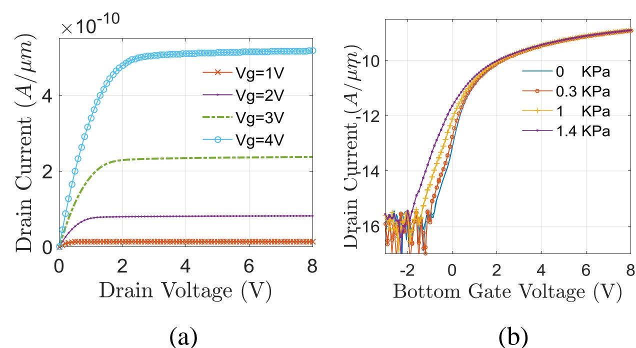
II. Results and Discussion

Fig.1 (a) shows the device structure which is composed of a layer of piezoelectric thin film biasing the top gate of the dual-gate a-Si:H TFT. In this paper, the TCAD simulation of the device is based on a TFT with W/L ratio of 100 μm /20 μm. Different from conventional operation of TFT in either OFF state or ON state, a subthreshold operation is implemented to improve the sensitivity of the device. Fig. 1 (b) shows how the conduction energy band of the cross section c-c in Fig.1 (a) bends in response to the force induced charge simulated by using Silvaco TCAD. When the device is biased in the subthreshold region, the band bending at the interface of top gate insulator and top surface of a-Si:H channel would lead to a significant increase of output current as a result of exponential decrease of the top channel resistance. Fig. 2 plots the TCAD simulation of the output characteristics and transfer characteristics of the device with and without forces. The transfer characteristics indicate that operation in the subthreshold region gives the highest sensitivity compared with linear and saturation regions. In this work, we plan to detail the simulation of this device upon various forces and its behavior in the subthreshold operation. Different dynamic input pressure from 0 KPa- 1.4 KPa has been simulated as plotted in Fig. 2 (b). An integrative device with patterned PVDF film laminating to the dual-gate TFT will be fabricated and characterized along with measurements on sensitivity and noise.



(a) (b)

Figure 1. (a) Device structure of a single pixel of tactile sensor; (b) Conduction band bending of the dual gate TFT



(a) (b)

Figure 2. (a) Simulated output characteristics of the TFT; (b) Simulared transfer characterristcs of the TFT upon various forces applied.

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Low voltage organic TFTs based on high-k/low-k dielectrics

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In the past decades, solution-processed organic thin film transistors (OTFTs) have been continuously studied due to their potential for electronic applications. OTFTs fabricated with conventional dielectrics, such as SiO_2, are usually of high operation voltage [1]. To reduce the operation voltage, various high-k dielectrics have been widely studied. Among the candidates, zirconium oxide (ZrO_2) is one of the most promising materials due to its wide band gap (5.8 eV), high dielectric constant (~25) and good thermal stability [1-5]. In previous studies, low temperature fabrication of ZrO_2 films can be realized by combing thermal annealing with UV photo-annealing [3].

In this study, we used solution-processed zirconium oxide films for high-k dielectric layers to fabricate low voltage, high performance organic thin film transistors (OTFTs). The ZrO_2 thin films annealed at 400 ℃ in ambient show a smooth surface, low leakage current density (3.93×10^{-7} A/cm^2 at -4V) and high capacitance (~348 nF/cm^2) (Fig.1). OTFTs based on the high-k ZrO_2 dielectrics were demonstrated. The resulting OTFTs show high mobility (~2.46 cm^2/Vs) and an on/off ratio of (~1.42×10^5), but with noticeable hysteresis (Fig.2.a).

To modify the surface, we fabricated OTFTs with different low-k modification layers, demonstrating high-k/low-k bi-layer dielectrics. Also, we investigated the effects of bulk capacitance and interfacial dipoles on the charge transports in organic semiconductor. The OTFTs with hexamethyldisilazane (HMDS)-treated ZrO_2 shows higher carrier mobility (~4.38cm^2/Vs), on/off ratio (~3.34×10^5), but the hysteresis does not improve (Fig.2.b). To reduce the hysteresis, we modified the OTFTs with polymethyl-methacrylate(PMMA)-coated ZrO_2, showing negligible hysteresis than those with bare ZrO_2 or HMDS- ZrO_2, also maintaining high carrier mobility (~3.45cm^2/Vs) (Fig.2.c). The ZrO_2/PMMA layers not only eliminate the defects but also help to reduce the high density dipoles near the interface between the dielectric and organic semiconductor, benefiting the charge transport in organic semiconductors.

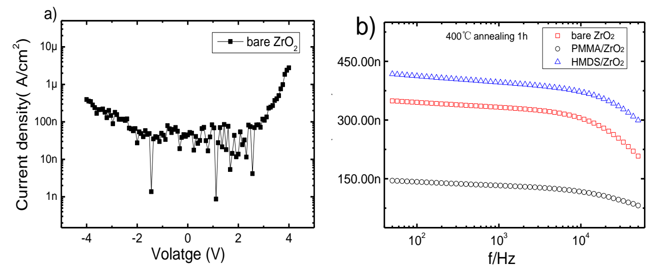

Fig. 1. Electrical properties of ZrO_2 dielectrics: a) current density versus gate voltage of bare ZrO_2; b) C-f measurement of different dielectrics.

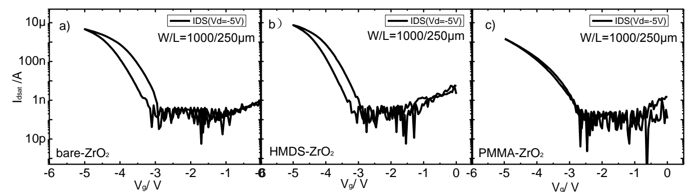

Fig. 2. Transfer characteristics of C8-BTBT TFTs based on: a) bare ZrO_2, b) HMDS/ZrO_2 c) PMMA/ZrO_2

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Solution Combustion Synthesis of Alumina Gate Dielectric using Hydrogen Peroxide/Water Solvent

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***Abstract*—In this paper, we demonstrate the solution combustion synthesis of alumina gate dielectric using for the first time with hydrogen peroxide (H_2O_2)/water (H_2O) solvent precursor. Due to the incorporation of H_2O_2 in the redox reaction, the leakage current is greatly decreased and the breakdown voltage is well improved by comparison with which synthesized using 2-methoxyethanol (2-ME) and water-based precursors.**

Keywords—Alumina;combustionsynthesis;hydrogen peroxide;

I. INTRODUCTON

High-k gate dielectrics such as alumina (Al_2O_3), ZrO_2, HfO_2 recently have been further reported with sol-gel process for solution processed TFT applications. In order to lower the highly external temperature, combustion process providing huge localized energy by self-igniting has been investigated. Usually, in the combustion synthesis process, 2-ME as the solvent, Acetylacetone (Acach) as the fuel are used. Those organic additives may greatly induce incomplete-igniting organic radicals, which influence the performance and the stability of thin films. Hydrogen peroxide is reported to be efficient addictive restraining those instabilities in sol-gel process without additional process. In this paper, we explore the multiple effects of hydrogen peroxide more than the addictive in combustion process, hence propose an advanced synthesis by employing peroxide (H_2O_2)/Water (H_2O) as both solvent and main reactant to fabricate purer alumina gate dielectric. The physical and electrical properties of the alumina thin film are investigated.

II. EXPERIMENT

Precursor solution preparation: 0.2M Aluminum nitrate nonahydrateis dissolved in 2.5mL of 2-ME (Ⅰ) or deionized water (Ⅱ) or H_2O_2/H_2O(Ⅲ), respectively. Then 60mg urea and 110ul (28%) NH_3(aq) were added into the solution with appropriate amount of nitrate acid (68%) to dissolve the agglomerated precipitation. All the solution were stirred for 1h and filtered with 0.2um syringe filters.

Thin film fabrication: p-type silicon wafer used as substrate were cleaned by RCA SC1 process, followed by microwave plasma treatment for 15min in O_2 atmosphere. Then, the alumina thin films were spin-coated, followed by hotplate baking at 300°C for 30min. These processes were repeated 4 times to achieve an appropriate thickness. For MIS capacitance structure, Al electrode was evaporated on the top of the alumina thin films.

III. RESULT AND DISCUSSION

Figure 1 shows the current densities of alumina films fabricated by various solution precursors. By replacing 2-ME with deionized water, leakage current density (Precursor (Ⅱ)) at 2 MV/cm decreases to $4.2x10^{-6}$A/cm^2, as well the breakdown occurs at higher bias stress. This may result from the fewer organic remains, carbon species for example. Moreover, the leakage current is further improved by using H_2O_2/H_2O-based synthesis. The lower leakage current of $1.12x10^{-7}$A/cm^2 has been observed at an electric field of 2MV/cm and the breakdown electric field is as high as 4.8 MV/cm. Considering the alumina refractive index changes from 1.62 to 1.65 and 1.71 for precursors (Ⅰ), (Ⅱ) and (Ⅲ), we suggested that using H_2O_2/H_2O-based precursor, the dense M-O-M networks are formed with higher uniformity, which inhibit the transport of the unwanted electrons. The improvement by addition of H_2O_2 to the precursor can be explained by two main effects: 1) more O_2 is provided by the synthesis itself with the decomposition of catalyst instead of ambient atmosphere; 2) H_2O_2 as oxidant aggravate the combustion process and the hydroxyl radials (OH*) released may further degrade organic residues.

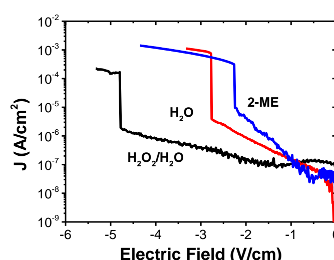

Figure 1

ACKNOWLEGMENT

This work is partly supported by the Science and Technology Project of Guangzhou City, China (No. 201505251254125).

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Effects of active layer thickness and annealing temperature of solution-processed InMgZnO thin film transistors

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Abstract—**The carrier-suppressing effect of Mg content in InZnO thin-film transistors (TFTs) was investigated using a sol-gel processed active channel. The TFT performance showed that saturation mobility of 0.11 $cm^2V^{-1}s^{-1}$, on/off ratio of 4.2×10^4, a threshold voltage of -1.82V.**

Keywords—InMgZnO; thin-film transistor; solution process;

I. Introduction

Compared with the traditional technology, the sol-gel method prossesses the characteristics of simple equipment, easy operation, adjustable solution components, and so on.

This paper researches the deposition of InMgZnO by sol-gel, for fabrication of thin film transistor, and focuses on the influences of active layer thickness(t_{active}), annealing temperature on the properties of InMgZnO TFT.

II. Experimental methods

A 0.3 M sol-gel solution of InMgZnO was prepared by dissolving $In(NO_3)_3\cdot xH_2O$, $Mg(CH_3COO)_2\cdot xH_2O$ and $Zn(CH_3COO)\cdot 2H_2O$ in 2ME.Atomic ratios of In:Mg:Zn= 5:1.7:2. The MEA was used as a stabilizer, and the molar ratio of MEA/Metal was fixed at 1. The solution was stirred at 65℃ for 2h.The bottom-gate and top-contact IMZO TFTs were fabricated on heavily doped p-type Si substrate as gate electrode with a 200nm thick thermally grown SiO_2 gate dielectric layer. A different active layer thickness was made by stacking multiple layers from prepared solution. After spin coating, the samples were post-annealed in air for 2h at at different temperature. Finally, metal Al layer was evaporated to form the source and drain electrodes with thermal evaporation system. The thickness of the Al layer was 100nm. The active width W and length L of TFT were 1000μm and 100μm.

III. Results and discussion

A. Different active layer thickness

Fig.1 shows transfer characteristics of solution-processed IMZO-TFT with different active layer thickness, and Table I concludes the corresponding electrical parameters. All the samples are N-active depletion-mode, and the properties are improved with the increase of t_{active}. This is contributed to the increased number of free carries in the channel region. The increased free carriers lead to the high flow of electrons to pass through source and drain,resulting in the increased off-current[1].But, When the active layer is too thick, it has many defects and traps capturing electrons. The defect scattering in connection with the trap charges increases with the increase of t_{active}[2], which deteriorates the properties of TFT. Thus, the optimal performance was obtained by 4 times of spinning. We measured the film thickness as 39 nm by ellipsometry.

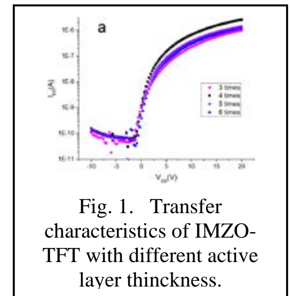

Fig. 1. Transfer characteristics of IMZO-TFT with different active layer thinckness.

TABLE I. Electrical properties of the Mg-doped IZO TFTs with various active layers thickness

times	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	on/off ratio	S.S (V/decade)
3	0.038	-3.03	2.5×10^4	0.95
4	0.111	-1.82	4.2×10^4	0.80
5	0.056	-2.12	1.4×10^5	0.88
6	0.049	-2.42	3.5×10^4	1.04

B. Different annealing temperature

TABLE II. Electrical properties of the Mg-doped IZO TFTs with different annealing temperature

temperature (℃)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	on/off ratio	S.S (V/decade)
350	NA	NA	1.89×10^3	1.38
400	0.032	-4.86	2.6×10^4	1.04
450	0.39	-5.15	5.2×10^3	2.55

Table II shows the electrical properties of TFT with different annealing temperature. when temperature is 400℃, the optimal performance is obtained.

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Laser annealing effects on the performance of InTiZnO thin film transistors

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Abstract

In this report, the excimer laser annealing (ELA) effects on the performance of InTiZnO thin film transistors (TFTs) were studied. By applying multiple irradiation pulses with low energy density, the InTiZnO TFT exhibited optimized electrical performance. The high bond strength of Ti-O makes InTiZnO thin films irradiated at low energy density more stable and stoichiometric, leading to the improvement of the device performance.

1. Introduction

Recently, amorphous metal oxide (AMO) thin films transistors (TFTs) have attracted considerable attention for transparent and flexible electronics due to their excellent physical properties, such as high mobility, high transparency, and low-temperature process in comparison with conventional amorphous silicon-based materials. AMO thin films deposited at low temperatures usually possess large number of defects and non-stoichiometric due to the existence of metal interstitials and oxygen vacancies. In order to improve the film quality and enhance the performance of the devices, post thermal annealing process with annealing temperature over 300 ^{o}C was usually applied during device processing. However, such high-temperature process would not be compatible with plastic-based TFTs. In order to explore the possibility of integrating with the flexible electronic devices based on plastic substrates, it is important to achieve high-performance TFTs with a low temperature process.

2. Discussion

In order to clarify the effect of ELA process on InTiZnO thin films, it is helpful to examine the thermal behavior of the thin film during the laser treatment. Using a simple analytical calculation, the transient temperatures of InTiZnO thin films depending on laser energy density were estimated, as shown in Fig. 1. The transient temperature (T) was given by $\Delta T= \alpha E/\rho C$, where α is the optical absorption coefficient; ρ is the mass density; C is the specific heat of the material. Note that the transient temperature of the InTiZnO thin films was calculated to be roughly 2000 ^{o}C when the laser energy density was 65 mJ/cm^2. Due to the sufficient short wavelength of the KrF excimer laser, the thin film can effectively absorb the laser energy. The calculated transient temperature of the InTiZnO thin films treated by KrF excimer laser was much higher than the previous reports. Meanwhile, the composition and/or structure of metal oxide thin films are susceptible to the ELA process.

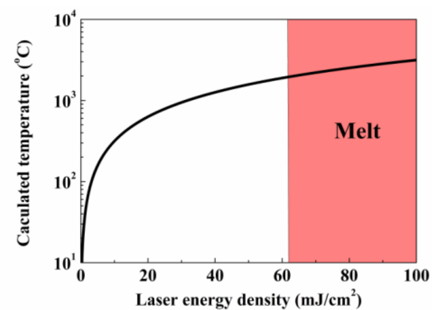

Fig. 1. Calculated transient temperatures of InTiZnO thin films as a function of laser energy density.

To realize the improved features of the ELA processed InTiZnO TFTs at low laser energy density, multiple irradiation pulses were applied. The transfer curves of the InTiZnO TFTs irradiated at 38 mJ/cm^2 with various pulses (1, 3, 5, and 6 pulses). The electrical performances of the TFTs were gradually improved with increasing the irradiation pulse, except for the TFT irradiated with 6 pulses. The InTiZnO TFT irradiated at the energy density of 38 mJ/cm^2 with 5 pulses exhibited the optimized electrical performance, including a $_{sat}$ of 6.8 cm^2 V^{-1} s^{-1}, an $I_{on/off}$ of 2.11×10^9, a V_{TH} of 1.9 V, and an SS of 0.17 V/dec. The degradation of the electrical performance of the TFT irradiated with 6 pulses is possibly due to the generation of porous structure in the bulk channel and/or the deterioration of interface between channel and dielectric. Note that the SS value of the TFTs was decreased from 0.21 to 0.17 V/dec with the increase of the irradiation pulse from 1 to 5. This trend is opposite to the InTiZnO TFTs irradiated with high laser energy densities. Meanwhile, these values are much smaller than most of the previous reports. This indicates that the multiple irradiation pulse process with low energy density is suitable for achieving TFTs with fast switching speed. Moreover, the small SS value also indicates the low density of trap states, which is also benefit to the devices stability.

Low-temperature, Nontoxic water-induced high-k zirconium oxide dielectric for fully-solution processed oxide thin-film transistors

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Abstract: The fabrication of water-induced amorphous high-k zirconium oxide (ZrO_x) dielectrics for thin film transistors (TFTs) has been proposed with the objective of achieving high performance and reducing costs for the next generation display. In this study, the as-prepared ZrO_x thin films were fabricated by a sequential process, including a UV-assisted photochemical treatment and thermal annealing process at temperatures lower than 300 °C. It is observed that the leakage current density of ZrO_x thin film decreases, and the capacitance increases with increasing annealing temperatures. To verify the application possibilities of ZrO_x thin films as the gate dielectric in complementary metal-oxide semiconductor (CMOS) electronics, both n-type In_2O_3 and p-type NiO_x channel layers were integrated on ZrOx dielectrics and their corresponding electrical performances were examined. The 250 °C-annealed In_2O_3/ZrO_x TFT exhibited a high electron mobility of 10.48 cm^2/V s, a small subthreshold swing of 100 mV/dec, a large on-off current ratio (I_{on}/I_{off}) of around 10^6, respectively. Moreover, the p-type NiO_x/ZrO_x TFT exhibited an I_{on}/I_{off} of 10^4 and a hole mobility of 5.7 cm^2/V s. It is noted that both n- and p-channel oxide TFTs on ZrO_x could be operated at voltages lower than 5 V. The low-temperature fabrication process represents a great step towards the further development of low-cost, all-oxide CMOS electronics on flexible substrate..

Keywords: water-inducement method; high-k ZrO_x dielectric; thin-film transistor; low-temperature process

1. Introduction

Metal oxide thin-film transistors (TFTs) have been extensively studied for large-area flat-panel display applications and sensor arrays over the past decade, because of their high carrier mobility, high transparency, excellent large-area uniformity, and reasonable electrical stability.[1] However, most of these oxide TFTs were integrated on conventional SiO_2 dielectric and thus operated at voltages higher than 30 V, which limit their applications in low power, portable electronics. Because the field-induced current is proportional to the charge accumulated, a reasonable technique to achieve low-voltage operation in TFT is to use high dielectric constant (k) material as the gate dielectric, which affords greater surface charge density at the semiconductor/dielectric interface. To overcome this bottleneck, various approaches have been explored to achieve large areal-capacitance gate insulators. Among these, inorganic high-k metal oxide dielectrics such as Y_2O_3, ZrO_x, Ta_2O_5, and Al_2O_3 are attractive candidates as these dielectrics simultaneously enable a low leakage current, through the use of a thicker film, as well as a low-voltage operation. In particular, ZrOx has been investigated widely due to its high dielectric constant of 25, relatively large band gap of 5.8 eV, and excellent thermal, chemical, and mechanical stability with Si. To date, ZrO_x thin films have been prepared by using various techniques such as atomic layer deposition, sputtering, e-beam evaporation, and solution process. Compare to vacuum-based techniques, solution process offers additional benefits: simplicity, low cost, high throughput, roll-to-roll capability, and the ability to fabricate a wide range of composition.

2. Dielectric and Electrical Properties of WI ZrO_x Dielectric

In this report, the thin film was fabricated on heavily doped p^+-Si/SiO_2 substrates by spin-coating ZrO_x precursor solutions. The key electric characteristics of the thin film are shown in Figure 1.

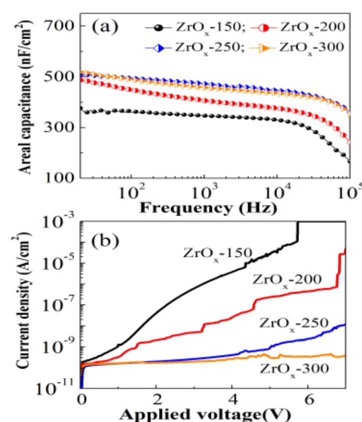

Fig.1.a) Areal capacitance and b) leakage current density of the ZrO_x dielectric.

Acknowledgement

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Solution-Processed Organic Field-effect Transistors with High Mobility and Excellent Uniformity

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***Abstract*—Organic thin-film transistors (OTFTs) based on indacenodithiophene-benzothiadiazole (IDTBT) semiconducting layer were fabricated by using both spin-coating and soft-blade coating. The devices showed high performance with high mobility (> 1 $cm^2V^{-1}s^{-1}$) and exhibited exceptional uniformity.**

***Keywords*—Organic thin-film transistors (OTFTs); solution processed; spin-coating; blade coating; uniformity**

I. Introduction

Solution processed organic thin-film transistors (OTFTs) have attracted much attention for its advantages of excellent flexibility and low-cost processing for large-area flexible electronics applications [1-2]. However, materials and processes for developing high performance OFETs of good uniformity are still of challenges. In this work, the donor-acceptor co-polymer semiconductor indacenodithiophene-benzothiadiazole (IDTBT) was deposited with different coating processes including spin-coating and blade-coating for OTFTs. It is found with both processed, high performance OTFTs with excellent uniformity can be achieved.

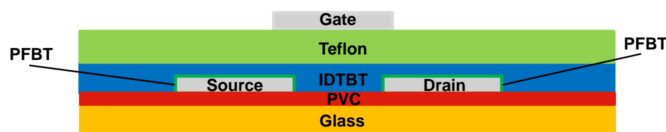

Fig. 1. Schematic of the cross-sectional structure of the fabricated top-gate bottom-contact OFETs.

II. Experiment

The OTFT devices were fabricated in top-gate bottom-contact (TGBC) structure illustrated in Fig. 1. The poly(vinyl cinnamate) (PVC) film was formed on the glass substrate by spin-coating as a buffer layer. Then, 40 nm-thick silver (Ag) source and drain (S/D) electrodes were deposited by thermal evaporation with a shadow mask to define a channel length of 55 μm and channel width of 1200 μm. The S/D electrodes were modified with perfluorobenzenethiol (PFBT) self-assembled monolayers (SAMs) before depositing the organic semiconductor layer. IDTBT in chlorobenzene were deposited by either spin-coating or blade coating, followed by annealing on a hotplate at 150 ℃ for 30 min to form the channel layer. Subsequently, a 404 nm thick Teflon film was deposited by spin-coating as the organic insulator layer. Finally, gate electrodes were defined by thermal evaporated of aluminum (Al) on top of dielectric layer through a shadow mask.

III. Results and Discussions

Fig. 2 shows the measured transfer curves of the fabricated 8 OTFT devices on a 2 cm × 2 cm substrate with the channel layer being deposited by spin-coating and blade coating, respectively. The devices all present high ON-OFF ratio (> 10^7) with excellent uniformity. The average mobility is 1.14 $cm^2V^{-1}s^{-1}$ for the OFETs with spin-coated IDTBT film and 1.41 $cm^2V^{-1}s^{-1}$ for the devices with blade coated IDTBT film.

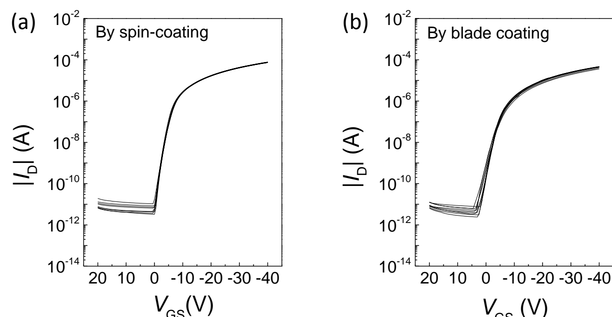

Fig. 2. The measured transfer curves of the fabricated 8 OTFT devices on a 2 cm × 2 cm substrate with the semiconductor layer being deposited by (a)spin-coating and (b)blade coating. (V_{DS} = -40 V)

IV. Conclusion

The donor-acceptor co-polymer semiconductor IDTBT being deposited by different processes including spin-coating and blade coating to achieve high performance OTFTs of excellent uniformity. Such uniform properties with large area scalable coating process will enable this material and device technology to be promising for constructing complex circuits.

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a-IGZO Thin Film Transistors with Offset Structure for Field Emitter Array Application

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***Abstract*—Amorphous indium-gallium-zinc-oxide thin film transistor (a-IGZO TFT) with offset structure is studied for active driving of ZnO nanowire field emitter arrays (FEAs). Simulated characteristics of the a-IGZO TFT with different offset lengths shows the feasibility of using the offset structure to control the maximum emission current. a-IGZO TFTs with offset structure were fabricated which integrated with ZnO nanowire FEAs and the experimental characteristics were analyzed using the simulated results.**

Keywords—a-IGZO TFT; FEAs; ZnO nanowires

I. Introduction

Large area ZnO field emitter arrays (FEAs) have potential application in X-ray source, field emission display, electron beam lithography, etc. [1]. By integrating thin film transistors (TFTs) with FEAs, one can achieve low driving voltage, precise control of current and stabilized emission current. Usually, in order to endure the high anode or control gate voltage employed in the device using FEAs, a high voltage device structure should be used. However, the fabrication process of the TFT should be compatible with that used for ZnO nanowire FEAs. a-IGZO TFT is considered as the ideal candidate for realizing above-mentioned purposes. In this study, a-IGZO TFT with offset structure was studied. Simulation of the a-IGZO TFT was carried out and a-IGZO TFTs integrated with ZnO nanowire FEAs were fabricated.

II. Device structure

In order to endure the high breakdown voltage required for FEA application, a high voltage a-IGZO TFTs with a drain-offset were adopted in this study. Fig. 1 shows the schematic of an a-IGZO TFT with offset structure. The a-IGZO TFTs has a bottom-gate, inverted-staggered structure. The operating voltage between drain and sources drops across the offset region of the channel. Therefore a the TFT can endure a higher drain-source voltage than a normal TFT.

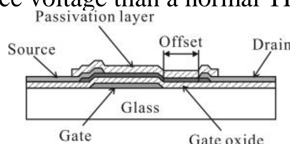

Fig. 1. Schematic of an a-IGZO TFT with offet structure

The devices characteristics with different offset lengths were simulated by device simulator ATLAS (Silvaco). The a-IGZO TFTs were fabricated on glass substrate using a process developed in our group and the process temperature was modified in order to make the fabrication process compatible with that for ZnO nanowire FEAs[2].

III. Results and Discussion

Fig. 2 shows the simulated transfer characteristics of an ideal a-IGZO TFT with different offset lengths. By assuming that the anode voltage is around 5kV in the FEA device, a drain voltage of 25V could be derived using the typical emission current of ZnO nanowire. It is clearly observed that the on-current is decreases as the offset length increases(inset of Fig.2). The results shows that by adopting offset structure, we can also better limit the on-current which help to improve the reliability of FEAs, avoiding possible current induced thermal run-away phenomena. Based on the simulation results, a-IGZO TFT was designed and fabricated. The experimental characteristics of the a-IGZO TFTs are compared with the simulated results.

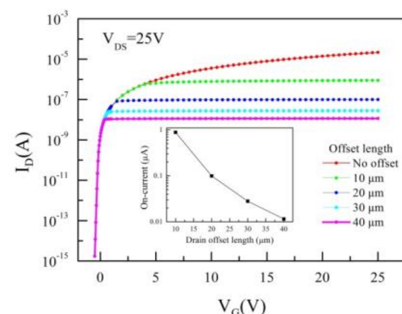

Fig. 2. Simulated transfer characteristics of the a-IGZO TFT.

IV. Conclusion

a-IGZO TFT with offset structure could help to achieve reliable low-voltage driving of ZnO nanowire FEAs.

Acknowledgment

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Simulation and study of Double-Material Gate TFT in order to reduce sub-threshold swing

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Abstract— In this paper, we propose a novel TFT structure which can reduce the subthreshold swing. The innovative idea is using *two different materials gate* which can increase the velocity of electrons and results in faster performance. Single and dual gate TFTs and also double-material gate TFT have been studied and compared. TCAD-SILVACO software is used to perform simulation. The results show that the double-material gate TFT drops below the threshold and its I_{off} is less than the conventional single and dual-gate TFTs. Sub-threshold swing is measured 1.2V/decade for single-gate single-material TFT, 0.54V/decade for single-gate double-material TFT , 180 mV/decade for dual-gate single-material TFT and 65mV/decade for dual-gate double-material TFT. Using of the double-material structure as gate in TFTs can decrease the sub-threshold swing by a factor of 2.2 in single gate and 3.1 in dual gate TFTs.

Keywords*— *TFT, dual material gate TFT, TCAD-SILVACO, dual gate TFT, single gate TFT

I. INTRODUCTION

Recently, TFTs are being used widespread in monitors in order to obtain high resolution colors. Unlike LCDs, in TFTs technology each pixel will switch with a separate transistor on the display so the image is more stable and without crosstalk.
One important issue in TFTs is decreasing the sub-threshold swing and consequently increasing the operation speed.
What has investigated in this paper is to compare the performance of conventional single and dual gate TFT structures with dual material gate TFT. Drain current vs. gate voltage curves of conventional TFT structures and dual material gate TFT in two-dimension have been compared with each other. The width of semiconductor is 20nm in all structures.

II. METHODES

In single material gate transistors, the electric field has one peak at drain end but in dual material gate transistors there are two peaks due to the electric field discontinuity at the junction of the gates, one at drain end and the other at the left gate end. This peak makes the electric field stronger at the source end which results in shorter effective gate length and increasing the velocity of electrons from source to drain. In the other words it will increase switching speed of transistor. Based on the above mentioned, the simulation of conventional and dual-material gate TFT structures will be discussed in the next section.

III. SIMULATION OF RESULTS

We have simulated conventional and dual material TFT structures and compared the results in this section. The simulation was done for single gate-single material and single gate-double material TFTs. It is clear that the use of two metals instead of one as a gate, where other parameters are the same, will decrease the subthreshold swing and I_{off}. For better understanding and proving this claim, the same simulation was done for dual gate-single material and dual gate-double material TFT structures. The results are shown in Figure1.

IV. CONCLUSION

By using two different materials with different work functions which are in connection with each other as the gate of TFT, subthreshold swing and I_{off} of the transistor will be decreased. This reduction represents the increasing of circuit's switching speed.

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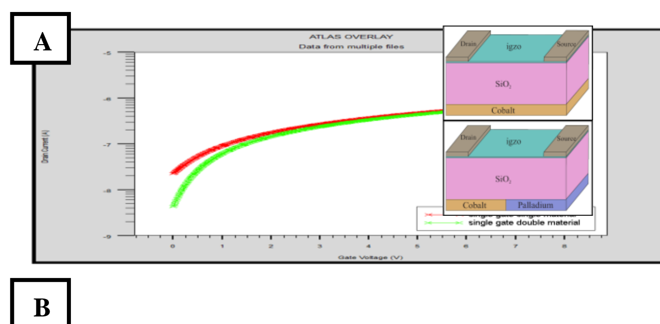

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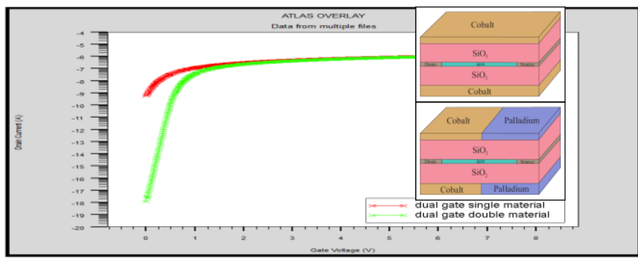

Fig. 1. A) subthreshold swing in single gate-single material and single gate-double material TFT structures-The thickness of semiconductor (igzo) is 20 nm. B) Subthreshold swing in dual gate-single material and dual gate- double material TFT structures-The thickness of semiconductor (igzo) is 20 nm.

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Temperature Dependent Gate Bias Stress Effect in Dioctylbenzothieno[2,3-b]benzothiophene (C8BTBT) Based Thin Film Transistor

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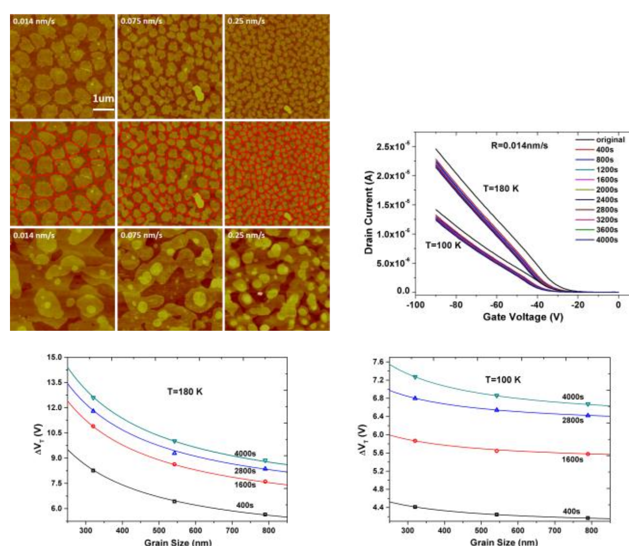
Bias stress effect (BSE), a phenomenon that threshold voltage shifts to the applied gate bias voltage, is a vital issue of the OTFT's operational instability. The origins of BSE have been generally attributed to charge trapping in deep localized states, in which carriers could hardly be released again within the time scale for charge transport in OTFT. In the previous research works, various factors were suggested to introduce deep localized states into OTFTs, including both intrinsic and extrinsic ones, such as bulk defects/impurities of active layer, dielectric layer induced disorder, contact resistance, environmental conditions including light exposure, presence of moisture et.al. When it comes to polycrystalline OTFT, imperfect molecules arrangements in grains boundaries would to a great extent affect the devices' stability. Former works have been done concerning about the relationship between the crystallinity of the organic active layer and bias stress effect in OTFTs. One unique feature in OTFTs is that, under the gate electric field, field induced carriers mainly distribute within a few nanometers with respect to the organic-dielectric interface. To further understand the relationship between initial layer's crystallinity and the electrical feature in the OTFT is of great essence.

We carried out a temperature dependent bias stress instability work on C8BTBT based organic thin film transistors below 200 K. Two-dimensional grains boundaries model (2DGB) was employed to analyze the correlation between bias stress effects and the morphologies of first monolayer of the organic film. This enabled us to study the contribution to the shifts of threshold voltage from both grains and grain boundaries by analyzing the temperature dependent characters. A negative correlation between threshold voltage shifts induced by traps distributed in grains and temperature was observed; while the shift of threshold voltages induced by traps distributed in grain boundaries took on a thermal activation character. These features suggested that the charge trapping rates might be limited by process of carriers' diffusion process in extended states and shallow trap states. This work may deepen our understanding of the bias stress induced threshold voltage shifts influenced by grains and grains boundaries respectively and be helpful to the optimization the designation of poly-crystalline OTFT.



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Field-effect Electroluminescence Spectra of Reverse-biased PN Junctions in Silicon TFT Device for Microdisplay

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***Abstract*—The emission of visible light by a monolithically integrated silicon p-n junction under reverse bias. The Silicon Light Emitting Devices (Si-LEDs) could be designed and realized utilizing the standard CMOS technology. Because of that, a fully CMOS integrated optical-type fingerprint sensor that use CMOS light emitting devices is achieved.**

Keywords—silicon LED, electroluminescence, microdisplay

I. Introduction

The PN junction LED based on breakdown radiation from "red spots," was reported in 1955 [1]. For silicon PN junctions reaching avalanching condition, visible electroluminescence emitting phenomenon is observed. Fig. 1 shows light generation mechanisms, also studied in more detailed [2].

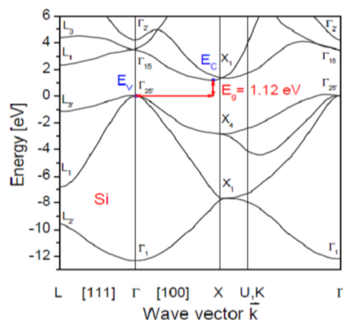

Fig. 1. Schematic representation of the calculated band structure of Si: possible photonic energy transitions

In the present work we study the spectral characteristics of thermionic emission in various structure in which the p-n junctions are reverse-biased.

II. Silicon LED for Microdisplay

Three different types of structures based on graded p-n junction are presented in Fig. 2.

Accordingly, it is shown in Fig. 3 that the normalized electroluminescence spectra of the three types of p-n junctions have the same emitting wavelength range [3].

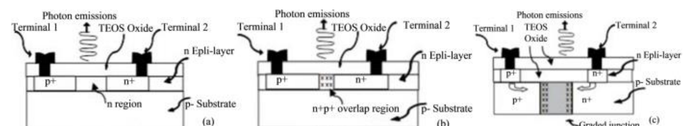

Fig. 2. Device design for testing light emission yield from device active regions with different structures: (a) p^+nn^+ Epi; (b) p^+n^+ overlap; (c) p^+nn^+ graded junction.

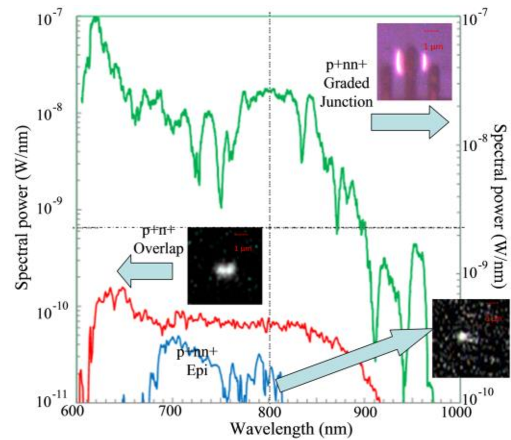

Fig. 3. A comparison between different device structures.

Acknowledgment

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Flexible Thin-film Transistors Fabricated on Plastic Substrate at Low Temperature

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***Abstract*—Fully-transparent Silicon-Zinc-Oxide (SiZO) thin film transistors (TFTs) have been successfully fabricated on flexible plastic substrate at low temperature. During sputtering the SiZO active layer, the device was prepared under 5% oxygen partial pressure exhibiting high performance with low threshold voltage V_{th} of 2.1V, small subthreshold swing (SS) of 151mV/decade, high saturation mobility µsat of $102cm^2V^{-1}s^{-1}$ and high current ratio I_{on}/I_{off} of 4.9×10^8.**

Keywords—SiZO; TFT; ; flexibilityg; low temperture

I. Introduction

The fabrication of thin-film transistors (TFTs) and other electronic device components on flexible substrate is a key technique to realize flexible electronics[1]. In-Ga-Zn-O (IGZO) is one of the most popular materials to fabricate TFTs with good performance [2]. However, Indium is rare and expensive. So it is necessary to find alternative oxide semiconductors with good characteristics.

In this paper, we developed Si-doped ZnO (SiZO) as the active layer. Here Silicon acts as a carrier suppressor due to higher bonding-strengths of silicon than that of zinc[3]. We investigated the electrical properties of 5% oxygen partial pressure SiZO TFTs and achieved high-performance characteristics.

II. Experiments

Staggered bottom-gate SiZO TFTs were fabricated by standard photolithography and lift-off technique, and are illustrated in Fig. 1 (a). Samples were prepared on PET plastic substrate at low temperature. When fabricating active layer, SiZO film was deposited by RF magnetron in 5% (pO_2/pO_2+pAr) oxygen partial pressure. The devices exhibit perfect flexible as shown in Fig. 1 (b).

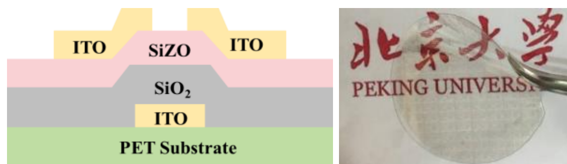

Fig. 1. (a) Cross-sectional schematic of the SiZO TFT device. (b) Picture of SiZO TFTs on a bent flexible PET substrate.

III. Results and Discussion

Fig. 2 shows the transfer characteristics of SiZO TFTs at 5% oxygen partial pressure. The extracted electrical parameters of SiZO TFTs with 5% oxygen partial pressure from transfer characteristics are demonstrated in Table I. For n-type oxide semiconductor, oxygen vacancy is important in conductivity mechanism because oxygen vacancy generates two free electrons in the conductor band and serves as a shallow donor. In order to switched off the device, when sputtering the active layer, 5% oxygen partial was introduced to decrease the excess carrier concentration and ensure the device can turn off with reasonable V_G.

TABLE I. TABLE I THE EXTRACTED ELECTRICAL PARAMETERS OF SIZO TFTS WITH DIFFERENT OXYGEN PARTIAL PRESSURE.

$O_2/Ar+O_2$ (%)	SS (mV/dec)	I_{on}/I_{off}	V_{th} (V)	μ_{sat} ($cm^2/V.s$)	I_{on} (mA)
5	151	4.9×10^8	2.1	102	0.36

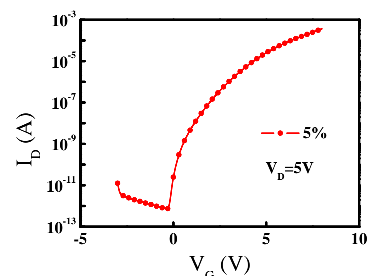

Fig. 2. Transfer characteristics of SiZO TFTs.

Acknowledgment

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Hybrid-Phase Microstructure in InSnZnO Thin Film and Its Application to High-Performance TFT

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***Abstract*—Indium-tin-zinc-oxide (ITZO) thin films with a novel hybrid-phase microstructure are introduced, where nanocrystals are embedded in an amorphous matrix. Following a sufficient study on microstructural and electrical properties of hybrid-phase ITZO thin films, top-gate thin-film transistors (TFTs) with optimal hybrid-phase ITZO channel are fabricated, and exhibit high electrical performance and stability.**

Keywords—Thin film transistor; ITZO thin film; hybrid-phase

I. Introduction

The advancement of displays towards large area and ultra-high definition claim thin film transistors (TFTs) with higher electrical performance, uniformity and stability. The most prevalent a-IGZO is theoretically limited by its composition and randomness, and seems insufficient to provide demanded mobility (> 20 cm^2/Vs) [1]. Binary ZnO suffer from instability issues that related to native defects [2]. In this paper, we propose the indium-tin-zinc-oxide (ITZO) thin film with less native defects, and introduce a novel hybrid-phase microstructure and provide relatively high mobility.

II. Experimental

The ITZO thin films were deposited by dc sputtering ITO target and rf sputtering ZnO target together. Based on the optimal co-sputtering conditions, top-gate TFTs with remarkable electrical performance and stability were also fabricated under 300 ℃. The substrates were 4-inch silicon wafers coated with thermal oxide. 80-nm-thick ITO was required as S/D electrodes. The ITZO films (50 nm) were deposited at room temperature, and patterned into active islands by wet etch. Next, 150-nm-thick PECVD-SiO_2 gate dielectric and 200-nm-thick Al gate electrode deposition was performed in sequence.

III. Results and Discussion

The blend of individually polycrystalline ITO and ZnO contributed to the formation of a hybrid-phase microstructure in co-sputtered films, where a number of nanocrystals survived and were embedded in an amorphous matrix, as shown in Fig. 1. Such hybrid-phase microstructure is believed to induce less sub-gap tail states, and higher theoretical mobility than those in amorphous phase because of lower atomic disorder. The transfer and output characteristics of the top-gate ITZO TFTs are shown in Fig.2. They exhibit relatively high electrical performance, such as field-effect mobility of 20 cm^2/Vs, subthreshold swing of 0.115V/dec, and on/off current ratio of 2×10^8. Fig. 3 presents the transfer curve evolution with 10 000 s for negative/positive bias stress (NBS/PBS) under dark, and almost no V_{th} shift is observed.

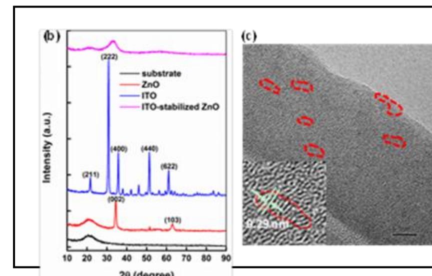

Fig. 1. XRD spectra and cross-sectional TEM of ITZO films

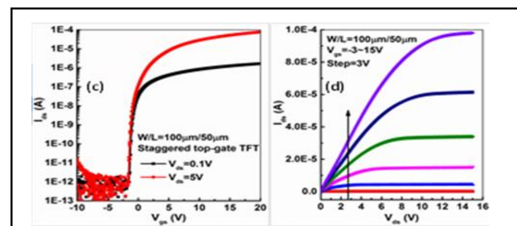

Fig. 2. Transfer and output characteristics of top-gate ITZO TFTs

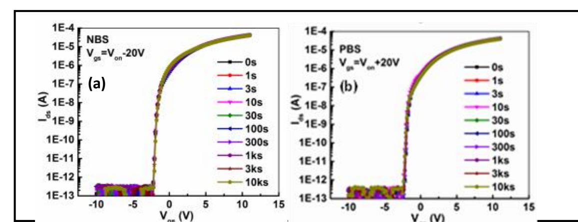

Fig. 3. Transfer curve evolution of ITZO TFTs for (a) NBS and (b) PBS

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Flexible Transparent Field-Effect Diodes Fabricated at Low-Temperature with All Oxide Materials

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***Abstract*—A flexible and fully transparent diode fabricated at low temperature (< 100 ℃) was reported with all oxide materials, using diode-connected thin-film transistor architecture. The diodes exhibited a high rectification ratio of 5 × 10^8 and low leakage current of 1 pA. Technology computer aided design (TCAD) simulation was employed to explore its working mechanism. Finally, a single-stage rectifier was demonstrated by applying this unique FED to rectify alternating current (AC) signals with different amplitudes and frequencies.**

Keywords—flexible; transparent; field-effect diodes; TCAD; rectifier

I. INTRODUCTION

Flexible transparent circuits have received more and more attention due to their tremendous applications in flexible displays, wearable human-machine interfacing devices, remote real-time health monitoring, implantable prosthetics, and multifunctional smart skins etc. To realize flexible circuits, flexible thin-film diodes (TFDs) are one kind of indispensable components similar to thin-film transistors (TFTs). In contrast to the remarkable progress made in flexible oxide TFTs during the last decade, very limited researches have been revealed on flexible oxide TFD, because most oxide semiconductors are n-type conductive and own large electron affinity (χ). In that case, it is hard to fabricate high-performance p-n or Schottky junction diodes based on these materials. Resolving this crucial issue, we report, to the best of our knowledge, the first flexible and fully transparent diodes fabricated at low temperature (< 100 ℃) with all oxide materials using diode-connected thin-film transistor architecture. The device is optically transparent with transmittance over 80% in visible spectra range and robust while mechanically bending up to r = 8 mm. Distinguished from other junction diodes, this diode follows field-effect principles as TCAD simulation reveals. The cathode serves as source, to eject electrons, while the anode both served as gate, to form conductive channel, and drain, to collect channel electrons, at the same time. The diodes exhibit high rectification ratio of 5 × 10^8 and low leakage current of 1 pA. Half wave rectification was achieved by a single-stage rectifier with a cutoff frequency of 1 MHz. To further increase the device performance, more investigations could be done to optimize the threshold voltage, subthreshold swing, crystalline quality, and device geometry.

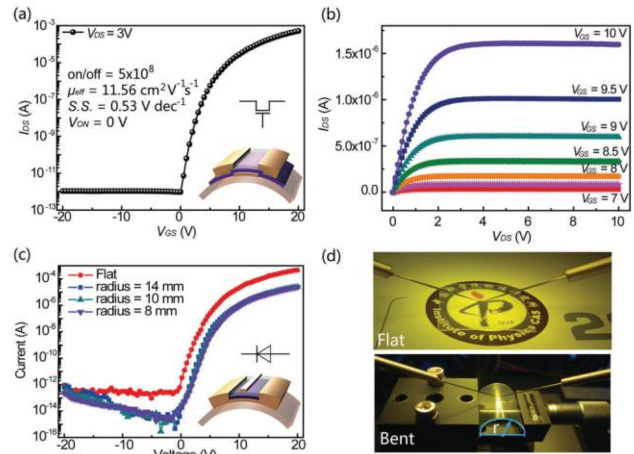

Fig. 1. *Electrical characteristics of referenced TFT and field-effect diode on PEN substrate. a) Transfer characteristics (I_{DS}–V_{GS}) and b) output characteristics (I_{DS}–V_{DS}) of referenced TFT. c) Current–voltage (I–V) characteristics of field-effect diode with a high rectification ratio of 5 × 10^8 while flat and bent. d) Photographs of devices under test.)*

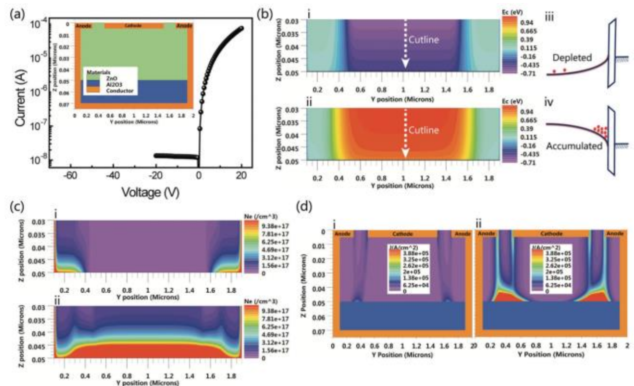

Fig. 2. *Simulation of electrical characteristics of field-effect diode under different voltage biases. a) Simulated I–V characteristics. Inset shows the defined device structure. b) Conduction band energy (E_c) distributions. E_c increased along cutline at V = −1 V (i), leading to a depleted channel (iii), while decreased at V = 1 V (ii), leading to an accumulated channel (iv). c) Electron concentration (N_e) distributions. N_e was cut down at V = −1 V (i), while boosted up at V = 1 V (ii). d) Current density (J) distributions. Negligible current was formed at V = −1 V (i), while clear current path formed at V = 1 V (ii).*

A Novel Three-Terminal UV PD on Barrier-Modulated Triple-Layer Architecture

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***Abstract*—We report a novel three-terminal device fabricated on MgZnO/ZnO/MgZnO triple-layer architecture. Because of the combined barrier modulation effect by both gate and drain biases, the device shows an unconventional I–V characteristics compared to a common field effect transistor. The photoresponse behavior of this unique device was also investigated and applied in constructing a new type ultraviolet (UV) photodetector, which may be potentially used as an active element in a UV imaging array. More significantly, the proper gate bias-control offers a new pathway to overcome the common persistent photoconductivity (PPC) effect problem. Additionally, the MgZnO:F as a channel layer was chosen to optimize the photoresponse properties, and the spectrum indicated a gate bias-dependent wavelength-selectable feature for different response peaks, which suggests the possibility to build a unique dual-band UV photodetector with this new architecture.**

***Keywords*—UV PD; field-effect transistor; PPC; barrier modulation; MgZnO/ZnO/MgZnO**

I. INTRODUCTION

The issues of how to improve the performance of ultraviolet photodetectors (UV PDs), such as suppressing persistent photocurrent (PPC) effect, are the main targets for all researchers. Based on the findings on a new bottom-gate ZnO/$Mg_xZn_{1-x}O$ heterojunction field effect transistor (HFET) on Si [1], we designed a new three-terminal UV PD using a MgZnO/ZnO/MgZnO triple-layer architecture [2]. The device shows a unique current-voltage (I-V) characteristics compared to usual FETs because of the modulated barrier by both gate and drain voltages. Photoresponse properties and working principles of this device were investigated and explored. The unique gate-bias control capability enables a new pathway to overcome the PPC problem. Additionally, structures with MgZnO:F as the channel layer were fabricated to extend the photoresponse performance, and the results indicate a new gate bias-dependent wavelength-selective response feature.

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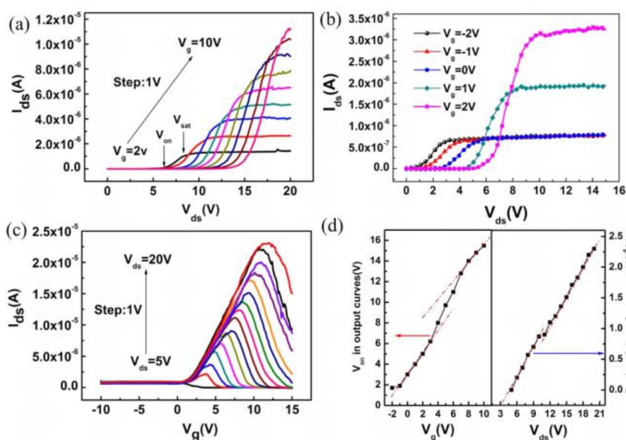

Fig. 1. *Novel I–V characteristics of our three-terminal device (a) I_{ds}–V_{ds} characteristics of MgZnO/ZnO/MgZnO/Si FET with V_g increased from 2 V to 10 V in a forward step of 1 V, (b) I_{ds}–V_{ds} characteristics conducted over a range of V_{ds} (0 ~ 15 V) and V_g (−2 ~ 2 V) (c) I_g–V_g characteristics as functions of V_{ds}, and (d) variation of the peaks in transfer curves and turn on voltages in output curves as a function of V_{ds} and V_g, respectively.*

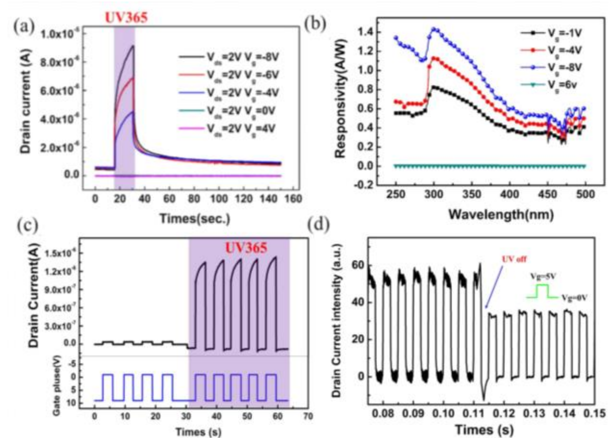

Fig. 2. *Photoresponse of novel three-terminal device (a) Drain–source current as a function of time as the device is subjected to a UV 365 nm light pulse at V_g varied in a range of 4 V to −8 V, (b) The room-temperature spectral responsivity of the MgZnO/ZnO/MgZnO/Si PD under different bias voltages, (c) V_{ds} was kept at 2 V bias to monitor the electrical and optical characteristics, while a continuous V_g plus was applied varied between −1 V and 9 V, and (d) suppression of the PPC when the PD is pulsed with positive gate bias.*