Fabrication of High-Performance Bridged-Grain Polycrystalline Silicon TFTs by Laser Interference Lithography

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***Abstract*— In this paper, bridged-grain (BG) low-temperature polycrystalline silicon thin-film transistors (TFTs) were fabricated. The periodic submicrometer BG structures were patterned using a maskless and large-area applicable laser interference lithography (LIL) technology, which was able to minimize extra manufacture costs of BG structures. Compared with conventional metal-induced crystallized (MIC) poly-Si TFTs, the BG-MIC TFTs involving the LIL technology exhibited reduced threshold voltage and subthreshold swing, improved ON–OFF current ratio, and suppressed leakage current and kink effect. Since the exposure energy density is one of key parameters for LIL, its relationship with device electrical performance was further investigated. It was found that when the exposure energy density was in the vicinity of 60 mJ/cm^2, these BG-MIC TFTs could perform optimally without device uniformity degradation.**

***Index Terms*— Bridged grain (BG), laser interference lithography (LIL), low-temperature polycrystalline silicon (LTPS), thin-film transistors (TFTs).**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon (LTPS) thin-film transistor (TFT) is regarded as one of the most promising backplane technologies to realize high-performance active-matrix flat panel displays (FPDs) [1]. In the LTPS technology, due to the better crystalline quality of recrystallized poly-Si film than directly deposited one, processes, such as solid-phase crystallization [2], metal-induced crystallization (MIC) [3], and excimer laser annealing [4], are proposed to convert a-Si into polycrystalline phase with fewer defects. However, poly-Si films suffer from high density and random distribution of grain boundaries (GBs) inevitably, as a result of polycrystalline phase. This will result in nonuniform and degraded electrical performance of TFTs across the panel. Therefore, it is necessary to mitigate the effect of GBs.

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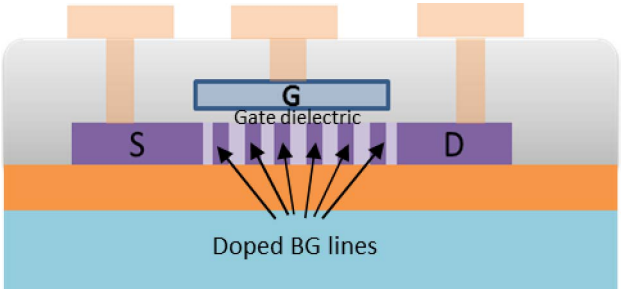

Fig. 1. Cross-sectional schematic of a BG-TFT.

In this paper, a bridged-grain (BG) structure is applied in MIC LTPS TFTs, which is beneficial to boost device electrical performance and uniformity. However, additional structures in TFTs mean the increase in manufacture costs. Therefore, the periodic submicrometer BG lines here are patterned using a maskless and large-area applicable laser interference lithography (LIL) technology, which is able to minimize extra costs. As an optical lithography technique, LIL exposure energy density is one of the key experimental parameters. Therefore, its relationship with the final device electrical performance is investigated. Meanwhile, considering device uniformity, an optimal LIL exposure energy density range can be defined.

II. Formation of BG Structure With LIL

A. BG Structure in LTPS TFTs

A BG structure (Fig. 1) consists of many heavily doped parallel BG lines, which are uniformly dispersed over length of the active channel. Thus, it divides the active region under the gate dielectric into a series of shorter subchannels. In terms of the dopant polarity in the BG lines, it should be the same as that in the source/drain (S/D) regions, whereas the dosage can be different.

The benefits brought by the BG structure can be summarized into three aspects. First, it is about a shortcut effect. The idea of a BG structure aims to link neighbor grains and suppress most GB barriers. In this case, when carriers enter into the conductive BG lines, they are able to choose those shortcuts provided by BG regions, so a large amount of GB barriers and traps along the transport path can be bypassed, leading to higher field-effect mobility ($\mu_{\rm fe}$) and steeper subthreshold swing (SS). Besides, the BG lines also divide the long poly-Si

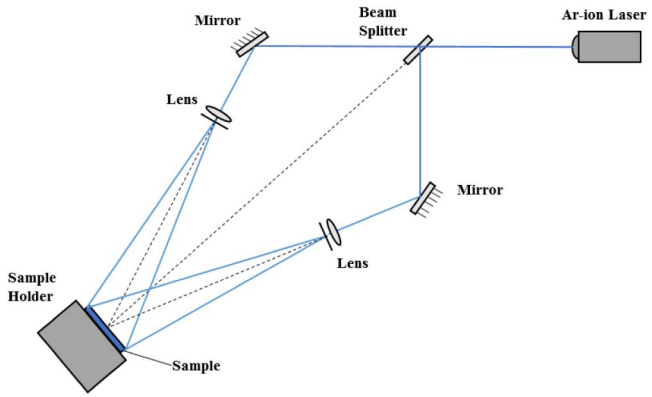

Fig. 2. Schematic of LIL system in the experiment.

active channel into many shorter subchannels. The accompanying short-channel effect will reduce threshold voltage (V_{th}) and increase ON-state current consequently, as well as bring severe drawbacks such as larger leakage current. However, for BG-TFTs, there is not only one single short channel, but a series of connected short subchannels. Therefore, the situation is different. The heavily doped regions form many junctions with their neighbor intrinsic poly-Si. The p-n multijunction structure relieves high electric field near the drain significantly and lowers down gate-induced drain leakage (GIDL) current in the OFF-state. Therefore, a multijunction effect is the third advantage of the BG structure [5].

Above all, it is illustrated that compared with conventional LTPS TFTs, all key electrical parameters, including V_{th}, SS, μ_{fe}, ON–OFF ratio and leakage current in BG-TFTs, can be improved [5]–[7].

B. LIL Technology

In order to pattern the periodic submicrometer BG structure, technologies, such as photolithography [5], LIL [6], and nanoimprint lithography [7], have been attempted already. Among them, the traditional photolithography is a common and standard choice. Nonetheless, it is mask based, and no specific photolithographic equipment is available for BG lines patterning in FPD industry. Hence, more investment needed is an issue both at research and early commercialization stage. On the other hand, since the BG structure is fortunately a periodic or quasi-periodic pattern, the LIL technology could be a relatively preferable inexpensive alternate, because it is maskless and large-area applicable.

As shown in Fig. 2, the LIL system in this paper is based on holographic interference [8]–[10]. The photosensitive layer on the surface of sample is exposed by the spatially periodic interference fringes, which are formed by two magnified coherent laser beams. The interference pattern period follows the equation:

$$\Lambda = \frac{\lambda}{2 \sin \frac{\theta}{2}} \tag{1}$$

where λ is the laser wavelength and θ is the angle between two laser beams. The laser source in this paper is an ultraviolet argon-ion laser with a wavelength of 363.8 nm. Thus, for a 1-μm pattern period, the corresponding angle θ is calculated as 20.96°. Since the photoresist (PR) is able to record the periodic interference intensity, a grating structure of the PR will remain on samples after developing. The regions covered by PR lines on the top will be prevented from the following ion implantation and keep intrinsic, whereas those exposed BG line spacing will become the main regions of heavily doped BG structure later on. Therefore, the BG lines are roughly defined. Notably, no mask is required across the process, and it is also promising for large-area backplane patterning.

In general, it can be divided into five major steps to form the BG structure: 1) spin-coating of antireflection coating (ARC) and PR; 2) defining BG lines with LIL technology; 3) develop and hardbake; 4) ion implantation; and 5) ARC and PR removal. Here, ARC between the substrate and the PR is necessary, because it can suppress the vertical standing waves formed by incident light and reflection light from the substrate surface, then keeping PR line edges smooth.

III. Device Fabrication

The process started from low-pressure chemical vapor deposition (LPCVD) of 45-nm-thick a-Si on 4-in p-type silicon wafer coated with 500-nm-thick thermal oxide. Then, about 1-nm-thick nickel silicide was sputtered on the surface of a-Si layer, which induced conversion from a-Si film to poly-Si film by the following nitrogen annealing at 600 °C for 10 h. After crystallization, nickel silicide was removed by sulfuric acid cleaning. Next, ARC and positive PR AZ1075 were spin coated on the surface of a poly-Si active layer in sequence, and then, PR was patterned into gratings with a period of 1 μm using the LIL technology. Since the aspect ratio (exposed area: covered area) would vary with the exposure energy (Fig. 3), the energy densities adopted in this paper were 0, 50, 60, 65, and 75 mJ/cm^2 to investigate the influence of LIL exposure energy density on electrical performance of eventual devices and find out the optimal value. After hardbaking, boron (B) implantation into the exposed regions was carried out with a dosage of 2×10^{15}/cm^2 and an energy of 23 keV. After ARC and PR removal, the BG lines were formed in the active channel, and no extra dopant activation process was needed. Then, the poly-Si layer was pattern into active islands using dry etch, followed by 50-nm-thick SiO_2 (LTO) deposition using LPCVD, and this Low-Temperature Oxide (LTO) served as gate dielectric. Afterward, a 300-nm-thick aluminum (Al) was deposited and patterned as gate electrodes, while S/D electrodes were formed by self-aligned B implantation with a dosage of 4×10^{15}/cm^2 and an energy of 25 keV. Subsequently, a 500-nm-thick LTO as a passivation layer was deposited, and contact holes were defined. A 700-nm-thick Al-1%Si layer was then sputtered and patterned as testing pads. Finally, the forming gas annealing was performed at 420 °C for 30 min.

IV. Results and Discussion

A. Comparison Between MIC and BG-MIC TFTs

Table I lists all key electrical parameters of the control MIC TFTs and BG-MIC TFTs fabricated with the LIL technology. Here, V_{th} is defined as V_{gs} when $|I_d|$ reached W/L $\times$ 10^{-7} A

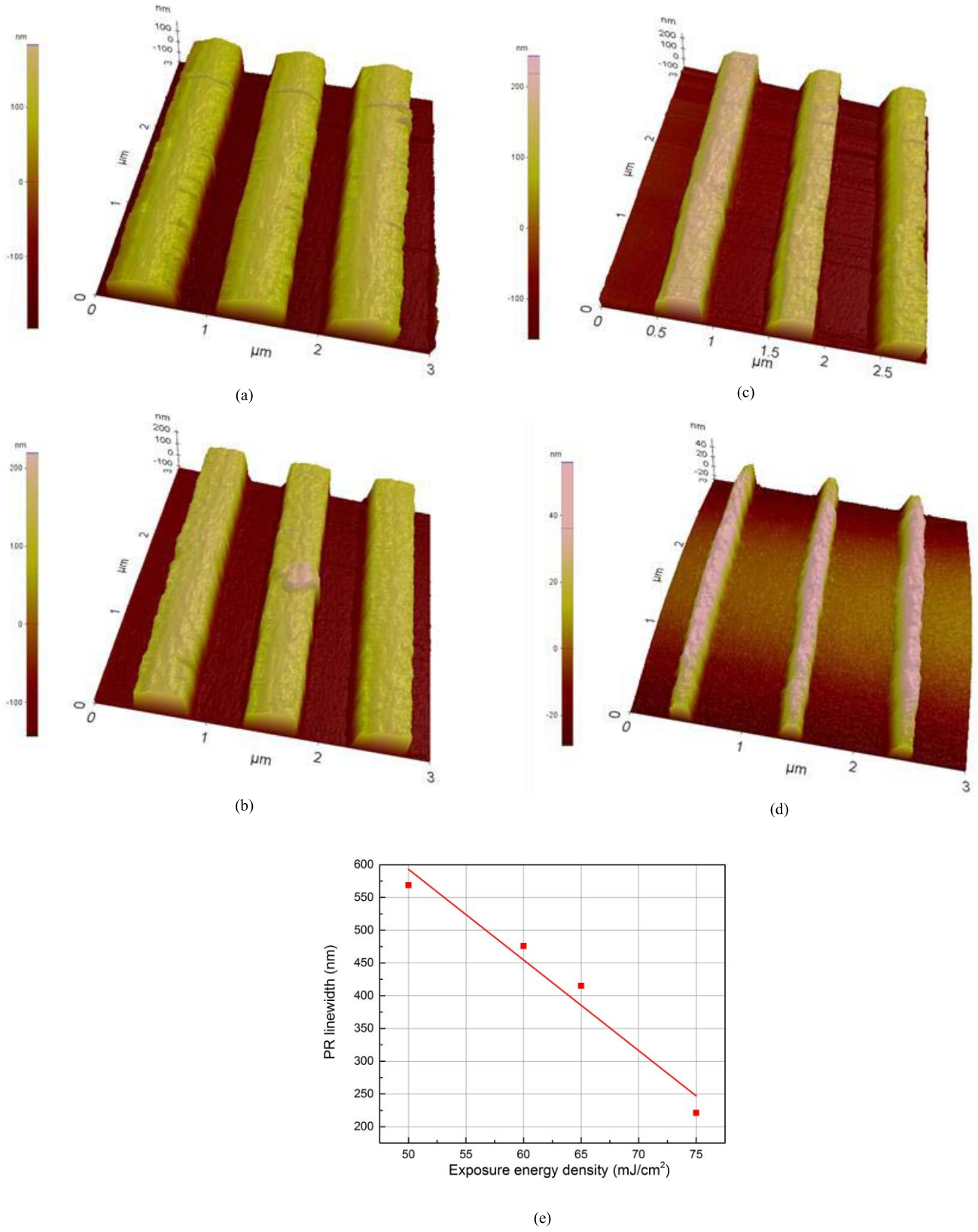

Fig. 3. AFM images of the exposed grating structures after LIL with the exposure energy density of (a) 50, (b) 60, (c) 65, and (d) 75 mJ/cm^2. (e) Plot of the remaining PR width (covered region) versus the exposure energy density and its corresponding fitted curve after LIL.

at $V_{\rm ds} = -5.1$ V, and the ON–OFF ratio is the ratio of the maximum and minimum values of $|I_d|$ at $V_{\rm ds} = -5$ V. Besides, GIDL current is equal to $|I_d|$ at $V_{\rm gs} = 5$ V and $V_{\rm ds} = -5$ V, divided by W. It can be seen that the electrical performance of BG-MIC TFTs is dramatically enhanced compared with the devices without a BG structure. $V_{\rm th}$ moves positively

TABLE I
ALL KEY ELECTRICAL PARAMETERS OF NORMAL MIC AND BG-MIC TFTS FABRICATED WITH THE LIL TECHNOLOGY

Key Parameters	MIC TFT	BG-MIC TFT	Definition
V_{th} (V)	-9.52	-5.08	V_{gs} when $\lvert I_d \rvert$ reached W/L×10^{-7} A at V_{ds}=-5.1 V.
SS (V/decade)	1.37	0.72	Slope of the log $\lvert I_d \rvert$ in 10^{-10} A range at V_{ds}=-5 V.
μ_{fe} ($cm^2/V{\cdot}s$)	23.51	104.51	$\mu_{fe} = \frac{L G_m}{W C_{ox} V_{ds}}$ at V_{ds}=-0.1 V.
On-off Ratio (×10^7)	0.297	4.21	The ratio of maximum and minimum value of $\lvert I_d \rvert$ at V_{ds}=-5 V.
GIDL (pA/μm)	7480	33.3	$\lvert I_d \rvert$ at V_{gs}=5 V and V_{ds}=-5 V, divided by W.

from −9.52 to −5.08 V, and SS drops to 0.72 V/decade. Due to the short-channel effect, the ON-state current of BG-MIC TFT becomes larger, whereas the leakage current indicated by GIDL current decreases by nearly 225 times. Thereby, the ON–OFF ratio increases to 4.21×10^7. In particular, benefiting from the BG effect discussed before, μ_{fe} increases from less than 30 to 104.51 $cm^2/V \cdot s$. The gate leakage current of the devices is below 10 pA. The transfer characteristics of control MIC TFTs and BG-MIC TFTs with the LIL technology are shown in Fig. 4(a).

Fig. 4(b) compares the output characteristics of MIC and BG-MIC TFTs. Except for the increased saturation current, it is observed that the kink effect in the saturation region can be suppressed significantly for BG-MIC TFTs. For a conventional LTPS TFT, when the voltage applied to the drain is high enough, extra electrons can be generated by impact ionization at the drain junction and flow toward the source contact in the back-channel region and it results in increased current in the saturation region, which is known as the kink effect [11]. However, owing to the multijunction effect in the BG structure, the high drain electric field can be relieved. Therefore, the BG structure is able to suppress the kink effect effectively in LTPS TFTs.

B. Optimal LIL Exposure Energy Density

As an optical lithography technology, LIL exposure energy density is one of most important parameters in BG line patterning. Similar to the situation in photolithography, excess exposure energy density can make more portion of positive PR dissolved during develop process, whereas the grating structure of PR may fail to be clearly patterned if exposure energy density is insufficient. Both situations will vary the remaining PR line width. Therefore, an LIL exposure energy density directly influences the electrical performance of BG TFTs.

As shown in Fig. 3, if the following ion implantation conditions keep fixed, with the increase in LIL exposure energy density, the PR line width left is gradually decreased. It is indicated that the separated submicrometer BG line spacing becomes narrower. Therefore, benefiting from the short-channel effect, devices with higher LIL exposure energy density exhibit lower $|V_{th}|$ and larger ON-state current.

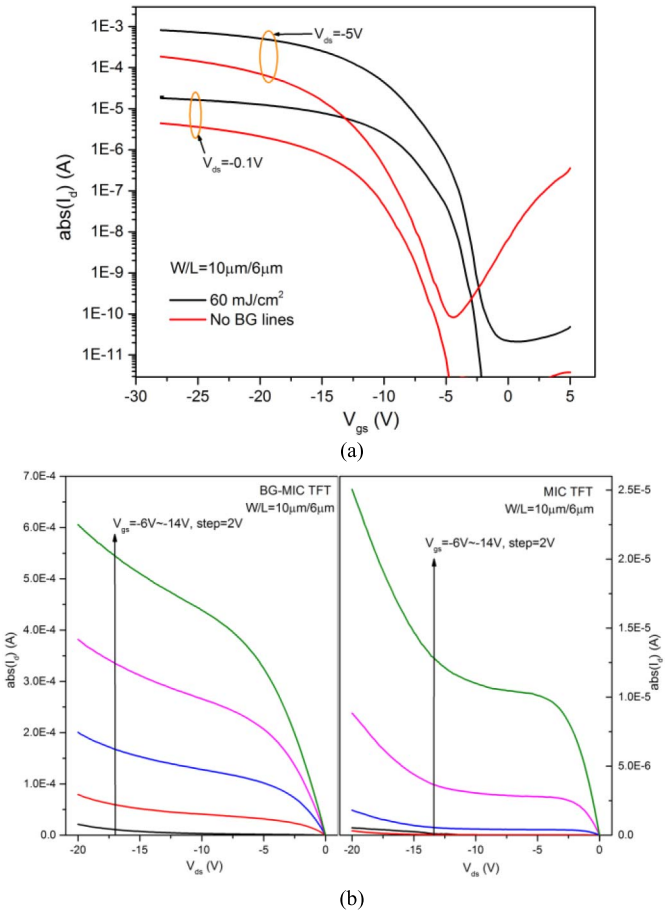

Fig. 4. (a) Transfer and (b) output characteristics of MIC and BG-MIC TFTs with the LIL technology.

Although the increase in leakage current can be suppressed by the multiple junctions across the active channel, it is hard to avoid when the BG regions expand, and the active channel becomes more and more conductive. Table II shows that there is an ON–OFF ratio peak in the vicinity of 60 mJ/cm^2. In addition, due to longer shortcuts provided, μ_{fe} can always keep increased when LIL exposure energy density ascends. However, considering the lateral scattering of B dopants during ion implantation process, it is sure that too high LIL exposure energy density is not preferable, because narrower BG line spacing will make the S/D of the TFTs short with each other, so that lose switching feature eventually. This is demonstrated in the case of 75 mJ/cm^2, where BG line spacing is too narrow, causing loss of the channel control by the gate. The detailed electrical performance can be referred to Table II, and the transfer characteristics of BG-MIC TFTs with different LIL exposure energy densities are exhibited in Fig. 5.

C. Device Uniformity

To investigate the spatial uniformity of our BG-MIC TFTs fabricated with the LIL technology, 50 TFTs uniformly distributed over each 4-in silicon wafer were measured. The results are shown in Fig. 6. It is clear that the BG structure can enhance the electrical performance of LTPS TFTs. The electrical performance and the uniformity of the devices are comparable with those using the conventional photolithography,

TABLE II

ALL KEY ELECTRICAL PARAMETERS OF BG-MIC TFTs FABRICATED WITH DIFFERENT LIL EXPOSURE ENERGY DENSITIES

Key Parameters	0 mJ/cm^2	50 mJ/cm^2	60 mJ/cm^2	65 mJ/cm^2	75 mJ/cm^2
PR line width (μm) (period=1 μm)	N/A	0.568	0.475	0.425	0.221
V_{th} (V)	-9.52	-6.04	-5.08	-1.87	
SS (V/decade)	1.37	0.75	0.72	1.7	
μ_{fe} (cm^2/V·s)	23.51	74.49	104.51	135.55	N/A
On-off Ratio ($\times 10^7$)	0.297	3.9	4.21	0.536	
GIDL (pA/μm)	7480	5.65	33.3	50600	

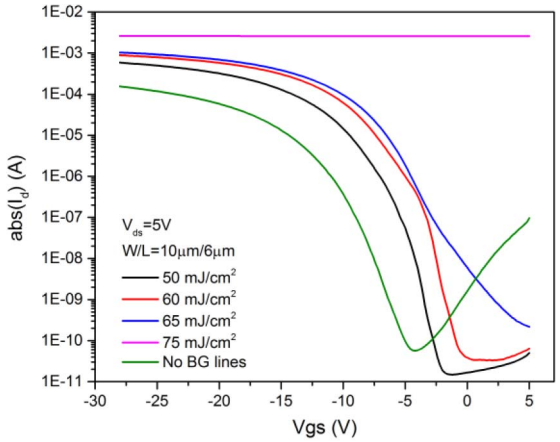

Fig. 5. Transfer characteristics of BG-MIC TFTs fabricated with different exposure energy densities.

as reported previously [5]. Besides, only if the LIL exposure energy density is in a reasonable range, TFT electrical performance uniformity can be well maintained. In particular, for parameters, such as GIDL current and ON–OFF ratio, their uniformities are greatly improved. Thus, the LIL technology with proper exposure energy density is not responsible for device nonuniformity. However, since the spots of two incident laser beams in LIL follow Gaussian power distribution, further increase in LIL exposure energy density may cause larger power variation among inference fringes, which will make a significant contribution to TFT electrical performance nonuniformity in the end. Therefore, if other conditions in this paper (for instance, ion implantation conditions) are fixed, the LIL exposure energy density maintaining relatively good device uniformity should be no more than 60 mJ/cm^2.

As discussed above, in the view of both device electrical performance and uniformity, it can be seen that 60 mJ/cm^2 is an optimal LIL exposure energy density choice in this paper. First, the BG-MIC TFTs fabricated with an LIL exposure energy density of 60 mJ/cm^2 exhibit improved electrical performance with an average threshold voltage V_{th} of -5.08 V, ON–OFF ratio of 4.21×10^7, and GIDL current of 33.3 pA/μm. Notably, the field-effect mobility μ_{fe} can reach as high as 104.51 cm^2/V · s. Moreover, the spatial uniformity for 50 uniformly distributed BG-MIC TFTs is also comparable with that of the conventional MIC TFTs.

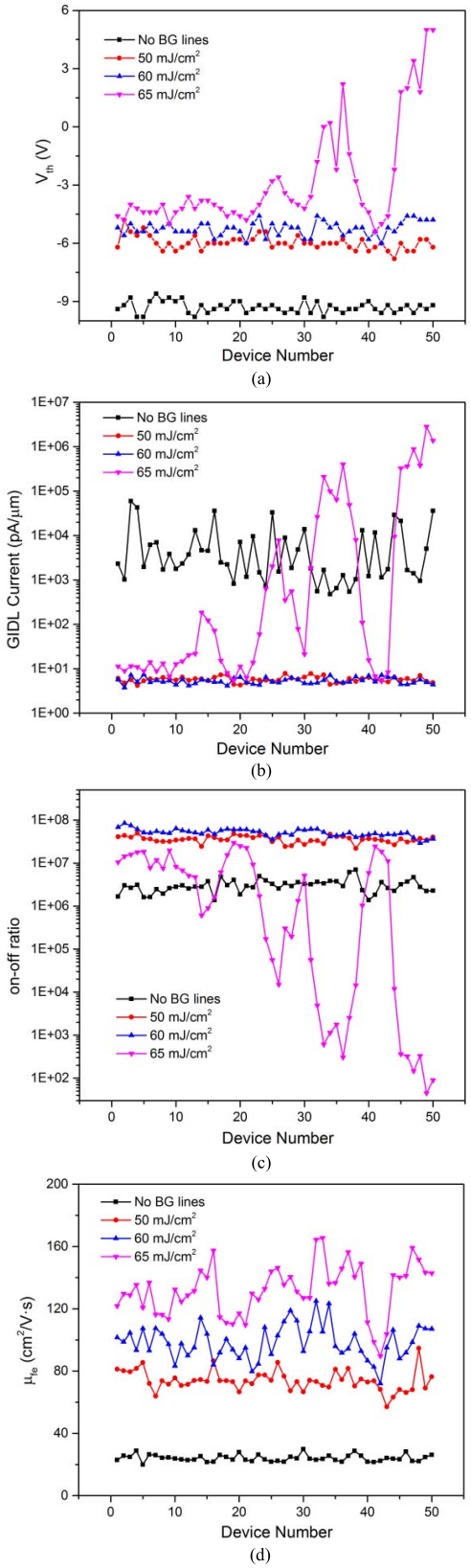

Fig. 6. Spatial electrical performance uniformity for 50 uniformly distributed normal MIC TFTs and BG-MIC TFTs with different LIL exposure energy densities. (a) V_{th}, (b) GIDL current, (c) ON–OFF ratio, and (d) field-effect mobility.

V. Conclusion

The BG structure is effective to improve the electrical performance of LTPS TFTs, and the BG-MIC TFTs were fabricated using an inexpensive LIL technology in the BG line patterning process. The relationship between the LIL exposure energy density and the device electrical performance was investigated. The optimal exposure energy density was found in the vicinity of 60 mJ/cm^2 when other conditions were fixed, as described in Section III. Furthermore, it was also demonstrated that the LIL exposure energy density no more than 60 mJ/cm^2 would not degrade the uniformity of LTPS TFTs.

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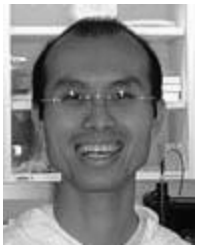

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