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High-performance staggered top-gate thin-film transistors with hybrid-phase microstructural ITO-stabilized ZnO channels

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In this paper, the ITO-stabilized ZnO thin films with a hybrid-phase microstructure were introduced, where a number of nanocrystals were embedded in an amorphous matrix. The microstructural and optical properties of thin films were investigated. It was found that the grain boundary and native defect issues in the pristine polycrystalline ZnO could be well suppressed. Meanwhile, such thin films also possessed relatively smooth surface and high transmittance in the visible range. Afterwards, the corresponding staggered top-gate thin-film transistors (TFTs) were fabricated at a temperature of 300 °C and exhibited fairly high electrical characteristics, especially with a field-effect mobility of nearly 20 cm² V⁻¹ s⁻¹ and a subthreshold swing as low as 0.115 V/decade. In addition, the electrical uniformity and the stability of devices were also examined to be excellent. It is expected that the staggered top-gate TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels are promising in the next-generation active-matrix flat panel displays. *Published by AIP Publishing.* [<http://dx.doi.org/10.1063/1.4966900>]

Recently, metal oxide (MO) semiconductors have drawn great attention as the thin-film transistor (TFT) channel materials. These MO TFTs present not only reasonable electrical performance and high optical transparency but also low processing temperature and production costs.¹⁻³ As a fundamental binary compound, the polycrystalline ZnO (pc-ZnO) is always attractive with medium electrical performance, and its earth-abundance provides the possibilities in low-cost applications. But, the pristine pc-ZnO TFTs suffer from severe instability issues related to native defects (such as oxygen vacancies (V_O) and dangling states) and grain boundaries.^{4,5} Thus, further optimizations are required, and the amorphous indium-gallium-zinc oxide (a-IGZO) is one of the typical solutions. Since reported in 2004, this multicomponent MO material rapidly becomes prevalent.⁶ However, with the advancement of active-matrix, flat panel display technologies towards the large area, ultra-high definition (UHD), and system on panel (SoP), a-IGZO seems difficult to provide TFT backplanes with the sufficient driving capability, because its mobility is theoretically limited by the composition and microstructure.⁷⁻⁹ On the other hand, the amorphous ZnON (a-ZnON) is proposed through substituting oxygen with nitrogen in the pc-ZnO, but the low reactivity between nitrogen and zinc gives rise to the long-term degradation of devices.^{10,11} Moreover, it is always controversial regarding whether the amorphous phase overweighs the nanocrystalline phase in MO semiconductors, particularly after the mobility limits of amorphous oxide semiconductors (AOS) are announced. Referring to most MO TFTs, their

best performance is actually obtained at the boundary between the amorphous and crystalline phases.⁹⁻¹¹

In this paper, we deposit a kind of ITO-stabilized ZnO thin films with a hybrid-phase microstructure, where a number of nanocrystals are embedded in the amorphous matrix. In comparison with the pristine pc-ZnO, it is believed that the microstructure together with the material composition can contribute to thin films with lower grain boundary and deep defect density inside. Then, our proposed thin films are employed as the channel layers of staggered top-gate TFTs. The corresponding devices exhibit remarkable electrical characteristics, uniformity, and stability, which are potential in next-generation active-matrix flat panel displays.

Generally, the individual ITO and ZnO thin films possess a polycrystalline microstructure even deposited at room temperature. When ITO and ZnO are blended together, it is likely to form a hybrid-phase microstructure in the mixture. Herein, the 2-in. circular ITO (90 wt. % In₂O₃ and 10 wt. % SnO₂) and the ZnO target were magnetron co-sputtered using a 120 W dc and 150 W rf power source, respectively. The base pressure was pumped to 3 × 10⁻⁶ Torr at first, and then the working pressure was set to 3 mTorr with the Ar/O₂ flow rate of 12/8 sccm. The microstructure of thin films was analyzed using X-ray diffractometer (XRD, PANalytical Empyrean) with Cu Kα radiation in the grazing incidence geometry. In addition, a high-resolution field emission transmission electron microscope (HRTEM, JEOL JEM-2010HR) and atomic force microscopy (AFM, Park XE150S) were also employed to do further microstructural characterization. All the thin films probed by AFM were deposited on the silicon wafers coated by 500-nm-thick thermally oxidized SiO₂. The substrate is extremely flat with a surface root mean square (rms) roughness of only 0.098 nm, which could less affect the

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surface morphology of the deposited thin films. The material composition of thin films was investigated using a X-ray photoelectron spectroscopy (XPS, Axis Ultra DLD), and the optical transmittance of thin films was measured by a UV-VIS spectroscopy (Perkin Elmer Lambda 20).

Afterwards, the staggered top-gate TFTs based on the hybrid-phase microstructural ITO-stabilized ZnO channels were fabricated. The processes started from 4-in. p-type silicon wafers coated with 500-nm-thick thermally oxidized SiO₂, followed by the formation of ITO source/drain (S/D) electrodes using the lift-off technique. A 50-nm-thick ITO-stabilized ZnO active layer was then co-sputtered and patterned into active islands by wet etch in diluted hydrofluoric acid. Since the co-sputtering conditions might affect the properties of thin films, it was required to tune them in order to achieve the best electrical performance of devices. After optimization, the oxygen partial pressure ratio (O₂/(Ar+O₂)) and dc/rf sputtering power combination adopted during deposition were 40% and 120/150 W, respectively. The channel width and length were designed as 100 μm and 50 μm, respectively. Next, the deposition of 150-nm-thick PECVD-SiO₂ as a gate dielectric layer and the definition of contact holes using dry etch were performed in sequence. A 200-nm-thick Al layer was then sputtered and patterned as gate electrodes and testing pads. Finally, the devices were annealed at 300 °C in air. Therefore, the whole processes were conducted at a relatively low temperature. The electrical characteristics of TFTs were measured in the probe station using a semiconductor parameter analyzer (Agilent 4156C).

The XRD spectrum of the ITO-stabilized ZnO thin films in Fig. 1(a) displays a relatively weak and wide peak between ITO (222) peak and ZnO (002) peak existing in the ITO-stabilized ZnO thin films. According to Scherrer's equation

$$D = \frac{k\lambda}{\beta \cos \theta}, \quad (1)$$

where D stands for the grain size, k is a constant (0.98), the incident X-ray wavelength λ is 1.540598 Å here, and β and θ

are the FWHM of the peak and diffraction angle, respectively.¹² Therefore, the estimated average grain size is about 1.5 nm, which indicates the existence of nanocrystals. Furthermore, the cross-sectional HRTEM image of thin films in Fig. 1(b) illustrates that a number of columnar nanocrystals are randomly distributed in the amorphous matrix. The lattice fringes with a measured interplanar crystal spacing of around 0.29 nm are surrounded by red-dash lines, and the grain size is consistent with the XRD-derived value. Moreover, compared to the pc-ZnO, fewer grain boundaries can be clearly observed. In other words, the grain boundary density in the ITO-stabilized ZnO thin films is diluted. The AFM images of the hybrid-phase microstructural ITO-stabilized ZnO and pc-ZnO thin films are shown in Fig. 2. Their rms roughness values are measured as 0.306 nm and 0.729 nm, respectively. It means that the hybrid-phase microstructural thin films with discrete nanocrystals possess more uniform and smoother surfaces than the pc-ZnO. Apart from the microstructural characterizations, the composition of the ITO-stabilized ZnO thin films is also investigated using the XPS technology. The portion of In, Sn, and Zn occupied among metal cations are found to be 38.64%, 2.66% and 58.70%, respectively.

Fig. 3(a) shows the optical transmittance (T) of the hybrid-phase microstructural ITO-stabilized ZnO thin films on quartz substrates. It is observed that such thin films are transparent in the visible range with an average transmittance exceeding 80%. Furthermore, the optical absorption coefficient (α) can be defined as follows:

$$T = (1 - R)^2 e^{(-\alpha d)}, \quad (2)$$

where T , R , and d represent the transmittance, reflectance, and the thickness of thin films, respectively. Herein, d is 110 nm. Then, the optical band gap (E_g) of thin films is derived. Theoretically, the relationship between α and the incident photon energy ($h\nu$) follows the Tauc model, which is given by

$$\alpha h\nu = \alpha_0 (h\nu - E_g)^n, \quad (3)$$

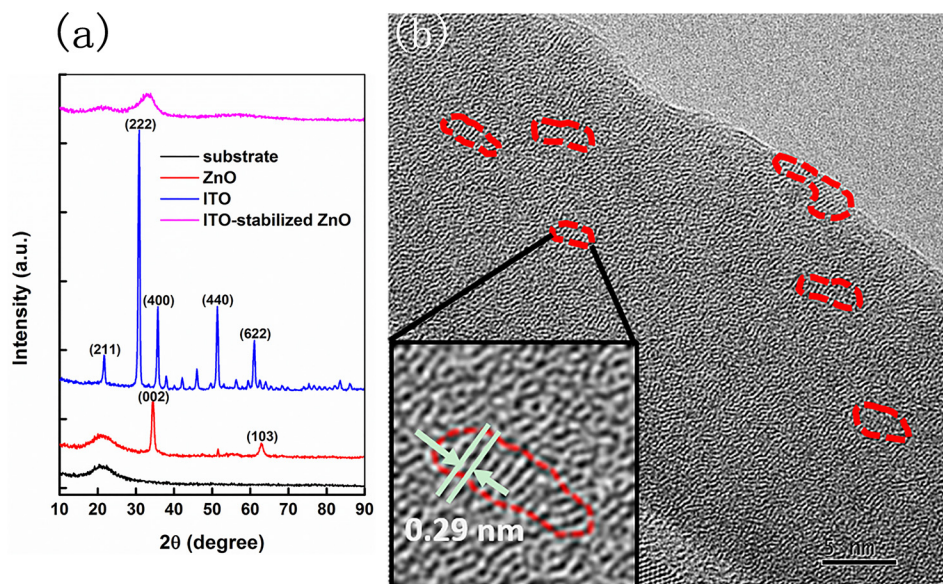


FIG. 1. (a) XRD spectra and (b) the cross-sectional HRTEM image of the hybrid-phase microstructural ITO-stabilized ZnO thin films, and the inset illustrates the nanocrystals highlighted by red-dash lines.

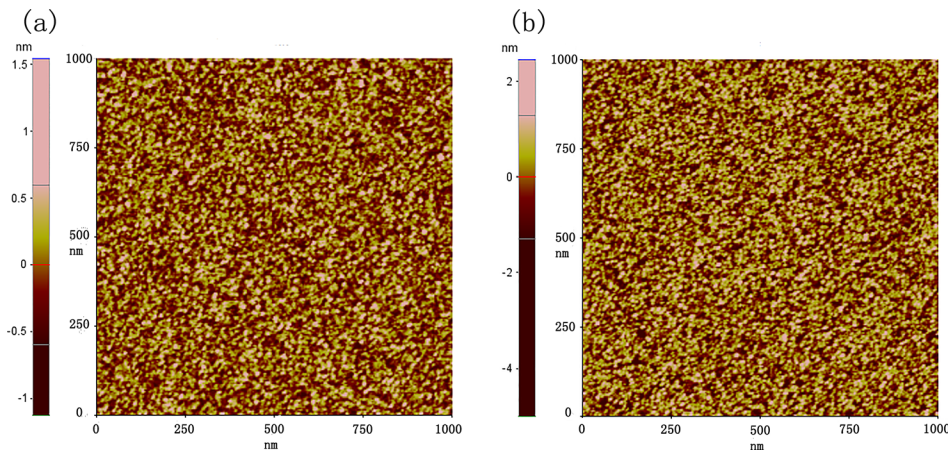


FIG. 2. The AFM images of (a) the hybrid-phase microstructural ITO-stabilized ZnO and (b) the pc-ZnO thin film surface.

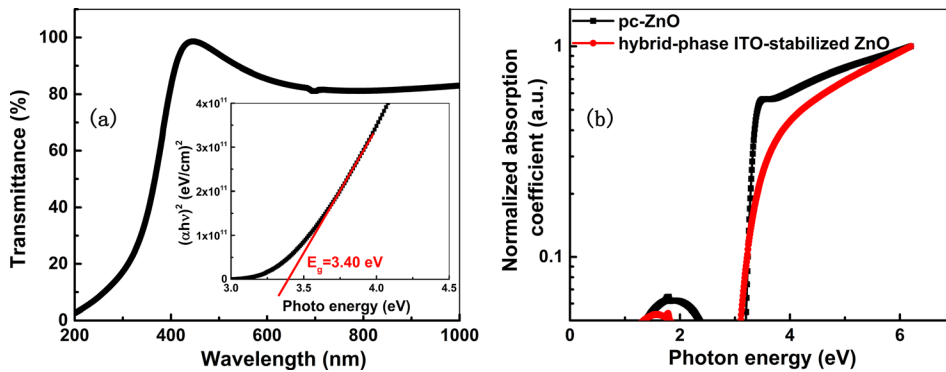


FIG. 3. (a) Optical transmittance of the hybrid-phase microstructural ITO-stabilized ZnO thin films. Inset: the plot of $(\alpha h\nu)^2$ as a function of $h\nu$. (b) Normalized optical absorption spectra of the hybrid-phase microstructural ITO-stabilized ZnO and pc-ZnO thin films.

where α_0 is an energy independent constant and n is the power factor of the transition mode.¹³ In this work, n is chosen as 0.5 for the ITO-stabilized ZnO thin films. Thus, E_g can be determined by extrapolating the straight line in the linear region of $(\alpha h\nu)^2$ versus $h\nu$ plot (see the inset of Fig. 3(a)). The result is equal to 3.40 eV. On the other hand, the normalized optical absorption spectra of hybrid-phase microstructural ITO-stabilized ZnO and pc-ZnO thin films are also plotted in Fig. 3(b). In both cases, there exists an absorption peak in the vicinity of 2 eV, and the hybrid-phase microstructural ITO-stabilized ZnO exhibits a smaller peak compared to the pc-ZnO. Since such peak is related to the deep defects like V_O in the sub-gap region of MO, it means the deep defect levels in the hybrid-phase microstructural ITO-stabilized ZnO thin films should be at a lower density.^{14,15}

The typical transfer and the output characteristics of the optimal hybrid-phase microstructural ITO-stabilized ZnO TFTs are plotted in Fig. 4. The transfer curves exhibit the relatively high electrical characteristics of the staggered top-gate devices. Herein, the field-effect mobility (μ_{fe}) can be obtained by transconductance (g_m) at a low drain voltage (V_{ds}), which is given by

$$\mu_{fe} = \frac{Lg_m}{WC_{ox}V_{ds}}, \quad (4)$$

where C_{ox} , W , and L are the gate insulator capacitance per unit area, channel width, and length, respectively. Thus, the derived μ_{fe} of devices can achieve as high as $19.10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at a V_{ds} of 0.1 V. It is believed that the diluted grain boundary

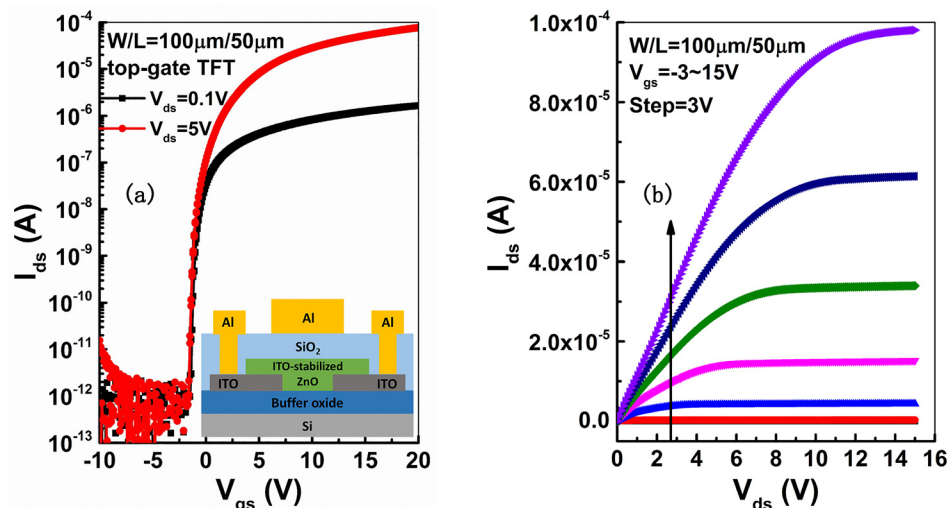


FIG. 4. (a) Transfer and (b) output characteristics of the hybrid-phase microstructural ITO-stabilized ZnO TFTs with staggered top-gate architecture. Inset: the schematic of staggered top-gate TFTs.

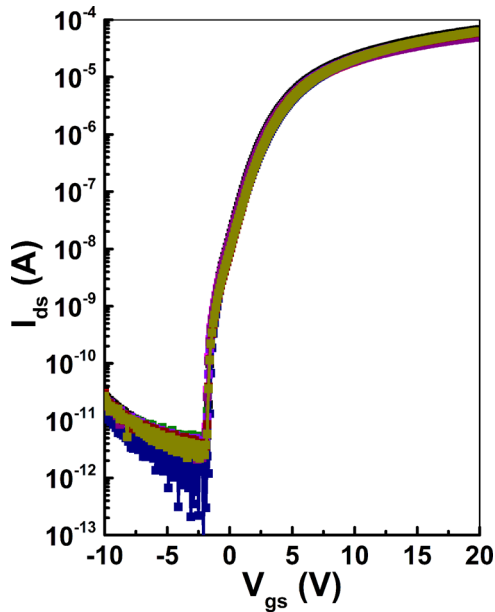


FIG. 5. Transfer curves of 15 hybrid-phase microstructural ITO-stabilized ZnO TFTs, which are uniformly distributed over a 4-in. silicon wafer to examine the electrical uniformity of devices.

density and In/Sn cation 5s orbital overlaps in the amorphous phase can provide the carrier percolation paths with low potential barriers, even though those large grains in the pc-ZnO are deteriorated into nanocrystals during co-sputtering process. In addition, the threshold voltage (V_{th}) and the on/off ratio of devices are -0.65 V and over 10^8 , respectively. In this work, V_{th} is defined as the corresponding gate voltage (V_{gs}) when the drain current (I_{ds}) reaches $W/L \times 10^{-8}$ A at $V_{ds} = 5$ V. Notably, the subthreshold swing (SS) is only 0.115 V/decade, which is much steeper than that in the pristine pc-ZnO TFTs. Moreover, the total trap density can be calculated using the following equation:

$$SS = \frac{qk_B T N_{total}}{C_i \log(e)}, \quad (5)$$

where q , k_B , and T are the electron charge, Boltzmann's constant, and absolute temperature, respectively; and C_i is the gate capacitance per unit area that here is determined by the dielectric constant and the thickness of PECVD-SiO₂. Thus, the total trap density is derived as low as $3.41 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. This verifies that the density of grain boundary and deep defect in the ITO-stabilized ZnO bulks are maintained at a low level;

meanwhile, the smoother surface of hybrid-phase microstructural ITO-stabilized ZnO thin films also contributes to a better channel/gate dielectric interface and reduced scattering in comparison with the pc-ZnO TFTs. The output curves illustrate a typical behavior of n-channel depletion mode TFTs. The clear pinch-off and the saturation of I_{ds} at high V_{ds} reflect that transistor channels can be effectively controlled by the gate and drain. However, there is a certain crowding effect observed at low V_{ds} , indicating the imperfect S/D contacts with high series resistance. This may partly restrict the electrical performance of devices.

Apart from the remarkable electrical characteristics, the hybrid-phase microstructural ITO-stabilized ZnO TFTs also present excellent device uniformity and electrical stability. Fig. 5 reveals the spatially electrical uniformity of staggered top-gate TFTs. There are 15 TFTs in total, examined over a 4-in. silicon wafer. It can be clearly seen that all the transfer curves shift within an extremely narrow range, which is comparable to AOS TFTs. One plausible reason is that the grain size of nanocrystals inside the hybrid-phase microstructural thin films is actually less than 2 nm. In the TFTs with the micrometer scaled channel length, these nanocrystals seem relatively small and sparse, and the diluted grain boundaries can be almost negligible. Therefore, the hybrid-phase microstructural ITO-stabilized ZnO TFTs provide a prominent solution for the next-generation flat panel displays, in particular, for the large-area OLED technologies.

On the other hand, the outstanding operation stability of TFTs under negative/positive gate bias stress (NBS/PBS) is shown in Fig. 6. The V_{ds} is kept at 5 V, and the applied V_{gs} for NBS and PBS are set to $(V_{on}-20)$ V and $(V_{on}+20)$ V for 10 000 s, respectively. Herein, V_{on} is the turn-on voltage, and corresponds to the V_{gs} at which the increase of I_{gs} could be clearly observed in a logarithmic I_{ds} - V_{gs} plot. The value for our devices is defined as -2.5 V. It can be seen that there is no stretch-out phenomena observed in the subthreshold region of transfer curves, implying the device degradation should be caused by charge trapping rather than defect creation. Furthermore, all the I_{ds} - V_{gs} curves of TFTs even without any passivation are almost overlapped during NBS and PBS tests. Considering the test step is 0.1 V, the V_{th} shifts in both cases are not more than ± 0.1 V. In addition, when the devices are double swept, no hysteresis phenomenon appears. This is attributed to the pretty high quality of the gate dielectric and the channel/dielectric interface, where the electron/hole trapping effects under gate bias can be well suppressed at room temperature.

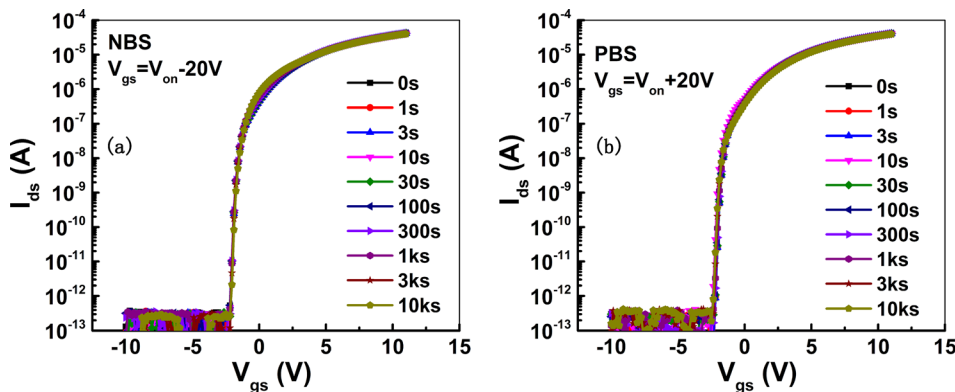


FIG. 6. Transfer curve variation of the staggered top-gate TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels under (a) NBS and (b) PBS test for 10 000 s. The transfer curve at every gate bias stress duration is double swept.

In summary, the ITO-stabilized ZnO thin films with a hybrid-phase microstructure were proposed, where a number of nanocrystals were embedded in an amorphous matrix. Then, the microstructural and optical properties of thin films were studied. The drawbacks such as native defects and grain boundaries in the pristine pc-ZnO thin films are found to be at a low density owing to such microstructures together with the material composition. Afterwards, the fabrication of corresponding staggered top-gate TFTs was conducted at a temperature of 300 °C, and the devices exhibited remarkable electrical characteristics especially with a quite steep SS of 0.115 V/decade. At last, the outstanding electrical uniformity and the stability of TFTs were also revealed. It is expected that the staggered top-gate TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels are promising in next-generation active-matrix flat panel displays.

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