Degradation Behaviors of Bridged-Grain Polycrystalline Silicon Thin Film Transistors under DC Bias Stresses

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Keywords: Reliability, Bridged-grain, Polycrystalline silicon, Thin Film Transistors, DC bias stresses

ABSTRACT

Device degradation behaviors of bridged-grain (BG) polycrystalline silicon thin films transistors (TFTs) under DC bias stresses are examined and analyzed. For self-heating stress, the reliability of BG TFT is better than that of normal TFT under the same stress power, which is likely attributed to the reduced grain boundaries resulted from BG line shielding effect. For hot carrier stress, BG TFT exhibits much more reliable characteristics compared to normal TFT, which is mainly due to the drain electric field reduction at drain side by BG lines. For negative bias temperature instability stress, on-current degradation of BG TFT is a little bit smaller than that of normal TFTs.

1. INTRODUCTION

Polycrystalline silicon (poly-Si) thin film transistors (TFTs) fabricated by the low temperature process have attracted much attention due to their great potential for system on panel (SOP) applications. To achieve the SOP integration, high performance poly-Si TFTs are desired and device reliability issue should be addressed. In the past decades, several methods, such as high-temperature annealing [1] and plasma treatments [2], have been developed to improve device characteristics. Recently a new technique named as bridged-grain (BG) method [3, 4], proposed by our group, is applied in the fabrication of low temperature poly-Si TFTs. By employing the BG structure, all device characteristics can be greatly improved. However, for this high performance BG poly-Si TFTs, the reliability issue is not studied yet.

For the reliability of poly-Si TFTs, it has been identified that self-heating (SH) effect [5, 6], hot carrier (HC) effect [6-8] and negative bias temperature instability (NBTI) effect [9-11] are three key mechanisms dominating the device degradation. In this work, degradation behaviors of BG poly-Si TFTs under SH stress, HC stress and NBTI stress are studied and analyzed. It is found that at the same stress power density, the SH reliability of BG TFTs are much more reliable than normal TFTs. Under the same HC stress and NBTI stress, the on-current (I_{on}) degradation of BG TFT is smaller than that of normal TFTs.

2. EXPERIMENTAL

The cross-sectional illustration and the top-down view of device structure are shown in Fig. 1a and 1b respectively. The fabrication process began with silicon wafers covered with 500 nm thick thermal oxide. First, 100 nm thick amorphous silicon was deposited by low-pressure chemical vapor deposition (LPCVD) as active channel layer. Then the crystallization process was carried out using either metal induced crystallization (MIC) method [3] or solid phase crystallization (SPC) method [4]. After crystallization, the photoresist was spin coated and then patterned into gratings with a period of 1 μm and the width ratio of 50%. Structure of the patterned photoresist captured by a scanning electron microscope (SEM) is shown in Fig. 1c. Boron ions were then implanted into the exposed areas of the poly-Si film. After implantation, the photoresist was removed and the BG lines were

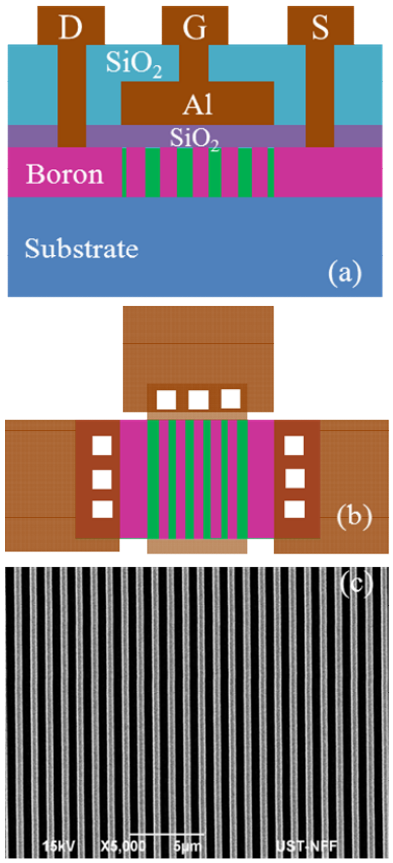

Fig. 1 (a) Cross sectional schematic view of device structure. (b) Top-down view of the device structure. (c) The SEM image of the structure of the grating.

formed. Then active islands were defined and patterned, followed by oxide deposition as gate dielectric. For SPC TFTs, the gate dielectric is SiO_2 while for MIC TFTs, the gate dielectric is SiO_2 or Al_2O_3. Next, 300 nm thick aluminum (Al) was sputtered and patterned as gate electrode. Then, self-aligned 35 keV boron implantation was done at a dosage of 4×10^{15} cm^{-2}. After implantation, 500 nm thick LTO was then deposited and contact holes were defined. 700 nm thick Al-1%Si was sputtered. After patterning the metal layer, the devices were sintered in forming gas for 30 min at 420 ºC. No further passivation was applied to these devices. Normal TFTs without BG lines are also fabricated at the same time for the comparison.

TFTs under test are 10 or 12 μm in channel length (L) and 10 or 12 μm in width (W). Three kinds of stresses, namely SH stress, HC stress and NBTI stress, are applied on both normal TFTs and BG TFTs, as shown in Fig. 2a, 2b and 2c respectively. Devices are measured before and after stresses by using the Agilent 4156A semiconductor parameter analyzer. Degradation is characterized by analyzing the field effect mobility (μ_{FE}) degradation or variation of I_{on}. The μ_{FE} is extracted from expression [4],

$$\mu_{FE}=\frac{LdG_m}{W\varepsilon_{ox}V_{ds}}$$

where d, ε_{ox} and G_m are physical gate dielectric thickness, gate dielectric permittivity and transconductance at V_{ds} = −0.1V.

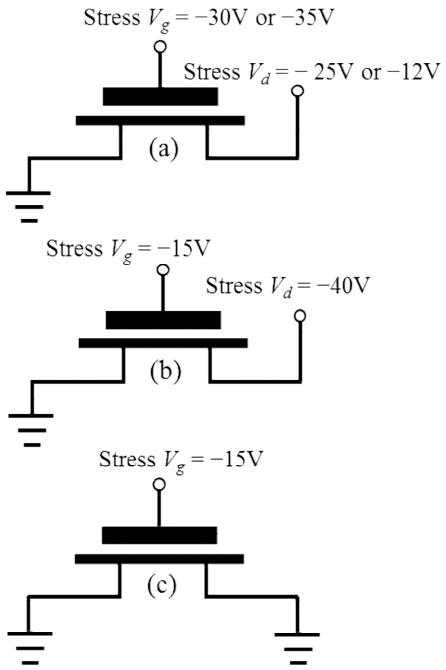

Fig. 2 (a) SH stress condition, (b) HC stress condition, (c) NBTI stress condition.

3. RESULTS AND DISCUSSION

3.1 SH Reliability

Shown in Fig. 3 is transfer curve degradation of normal TFT and BG TFT under SH stress at the same stress power density (0.04mW/μm^2). To obtain the same stress power density, different stress V_g and stress V_d are combined for normal TFTs (stress V_g = −35V, stress V_d =−25V and grounded source electrode) and BG TFTs (stress V_g = −30V, stress V_d = −12V and grounded source electrode). It can be clearly observed that BG TFT has much better initial electrical characteristics compared to normal TFT in terms of larger I_{on}, steeper sub-threshold swing and lower off-current. According our previous reports [3-4], these striking differences are caused by short channel effect and multi-gate effect in BG TFTs. At the same stress power density, BG TFTs exhibits more reliable SH reliability than normal TFTs. The SH degradation is mainly attributed to defect generation by distorting/breaking of strong Si−Si bonds at grain boundaries (GBs) [5]. Compared to normal TFTs, the GBs can be effectively shielded by the heavily doped BG lines in the channel for BG TFTs and thus SH effect could be alleviated.

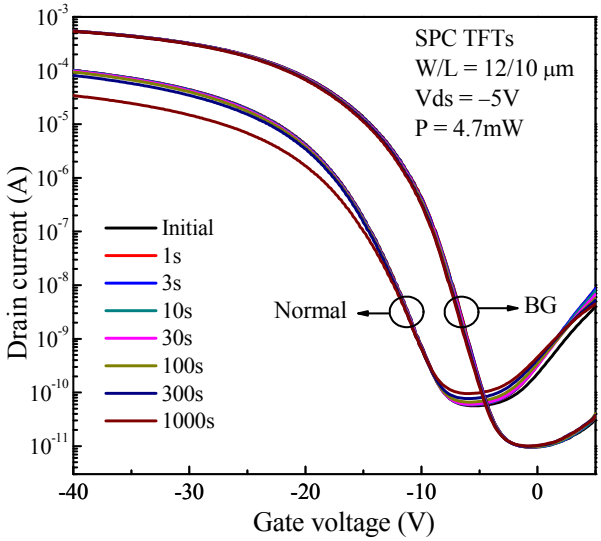

Fig. 3 Transfer curve degradation of normal TFT and BG TFT under SH stress with the same stress power.

3.2 HC Reliability

Shown in Fig. 4 is μ_{FE} degradation of normal SPC TFT and BG SPC TFT under the same HC stress, measured at V_{ds} = −0.1V. It is found that the μ_{FE} of normal TFT degenerate dramatically. For maximum μ_{FE}, it decreases from ~30.3 cm^2/Vs to ~0.3 cm^2/Vs after 10000s and the percentile degradations of maximum μ_{FE} is almost −100%. For BG TFT, under the same HC stress, the m-

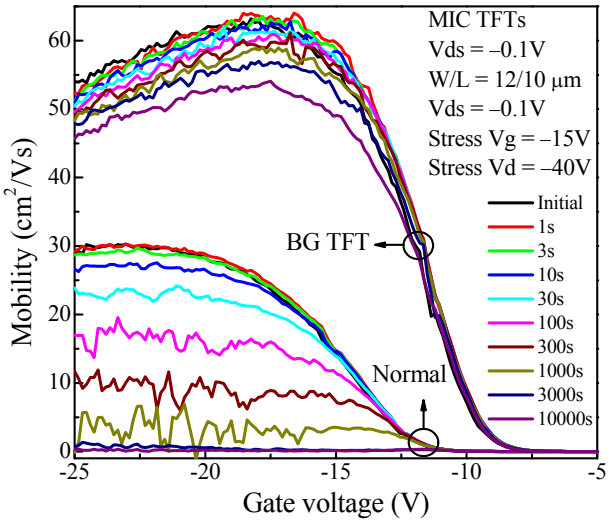

Fig. 4 Mobility degradation of normal TFT and BG TFT under HC stress.

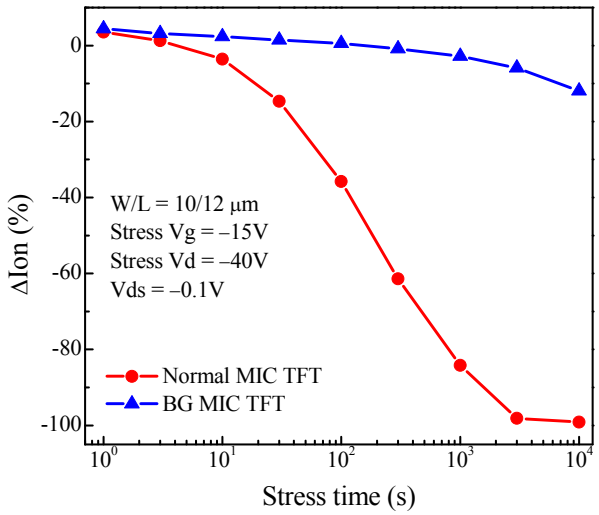

Fig. 5 I_{on} degradation dependent on stress time in normal TFT and BG TFT under HC stress.

-aximum μ_{FE}, decreases from ~63.2 cm^2/Vs to ~54.1 cm^2/Vs after 10000s and the percentile degradations of maximum μ_{FE} is only −14.4%. Shown in Fig. 5 is I_{on} degradation dependent on stress time in normal TFT and BG TFT under HC stress. Consistent to μ_{FE} degradation, I_{on} degradation of BG TFT is much smaller than that of normal TFT. It can be considered that the improved HC reliability in BG TFTs is mainly due to the lateral electric filed reduction caused by BG lines at drain side.

3.3 NBTI Reliability

NBTI stress induced degradation in normal TFTs and BG TFTs are also examined. Shown in Fig.6 is the I_{on} degradation dependent on stress time in normal SPC TFT and BG SPC TFT under NBTI stress (stress V_g = −15V with grounded source and drain electrodes). It can be observed that the I_{on} degradation of BG TFTs is smaller t-

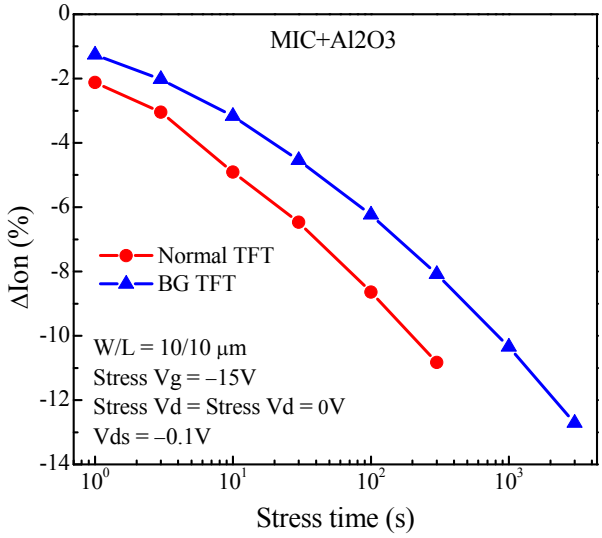

Fig. 6 I_{on} degradation dependent on stress time in normal TFT and BG TFT under NBTI stress.

-han that of normal TFTs. The NBTI degradation is mainly attributed to the generation of interface/grain boundary trap states and fixed oxide charges [9-11]. The smaller I_{on} degradation of BG TFTs may be attributed to the smaller grain boundary trap state density in the active channel of BG TFTs.

4. CONCLUSION

In this work, degradation behaviors of BG TFTs under DC bias stresses are studied and analyzed. Compared to normal TFTs, BG TFTs have much better SH reliability and HC reliability. The improved SH reliability is likely attributed to the BG line screened GBs and the improved HC reliability results from the drain electric reduction at drain side by BG lines. For NBTI stress, I_{on} degradation of BG TFT is a little bit smaller than that of normal TFTs, which may be attributed to decreased grain boundary trap state density caused by BG lines.

5. ACKNOWLEDGEMENTS

Authors would like to thank Prof. Mingxiang Wang in Soochow University for valuable discussions. This work was supported by Hong Kong Government Research Grants Council Theme-Based Research Scheme under Grant T23-713/11-1.

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