High-Performance Low-Temperature Polycrystalline-Silicon Thin Film Transistors with Submicron-Dot-Array Doped Active Channel

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Abstract

A novel method named as submicron-dot-array (SDA) doping is developed for the fabrication of low-temperature polycrystalline-silicon thin film transistors (TFTs). All electrical parameters are improved by employing SDA structure. It is worth mentioning that the mobility of fabricated device is 4 times of conventional TFTs. The proposed SDA method has great potential for system-on-panel applications.

***Keywords*:** Low-temperature polycrystalline silicon, thin film transistors, submicron-dot-array doping

1. Introduction

Low-temperature polycrystalline-silicon (LTPS) technologies are actively being developed to generate high performance thin film transistors (TFTs) for system-on-panel applications [1]. High-performance LTPS TFTs with low operating voltage, steep subthreshold swing (*SS*) and large on-state-current/off-state-current (I_{on}/I_{off}) ratio are desired to accomplish the above purpose. However, polycrystalline-silicon (poly-Si) thin film has numerous grain boundaries (GBs) inside [2-4], resulting in small field-effect mobility (μ_{FE}), poor *SS* and small I_{on}/I_{off} ratio in poly-Si TFTs and thus seriously limiting its application into driving circuits of active matrix displays. Several methods [5-7] have been proposed to reduce the GBs, such as high temperature annealing [5], plasma passivation [6] and bridged-grain (BG) technique [7]. For the high temperature annealing [5], the reported temperature often exceeds 700ºC, which is incompatible to LTPS technology. For the plasma passivation, it often brings process variation and reliability issues [6]. As to the BG technique [7], the BG lines are one dimensional and thus the device in the layout must be put in the specific position, which would sacrifice the circuit area and increase the difficulty for circuit designers. All methods above have critical shortcomings.

In this work, a new method named as submicron-dot-array (SDA) doping is proposed to improve device performance. The proposed SDA doping method is low temperature compatible, two dimensional and without process variation and reliability issues. With the SDA doping in the active channel, device shows great improvement in terms of μ_{FE}, *SS* and I_{on}/I_{off} ratio. It is worth mentioning that the μ_{FE} of the proposed TFTs with SDA doped channel is up to 58.4cm^2/Vs, which is 3 times larger than that of conventional poly-Si TFTs. The test results suggest that the proposed SDA method is suitable for system-on-panel application.

2. Experimental

The cross-sectional illustration of device fabrication process flow is shown in Fig.1. First, 500-nm-thick thermal oxide was grown on 4-inch c-Si wafers in furnace. Then, 100nm a-Si active layer was deposited by low-pressure chemical vapor deposition. Solid-phase-crystallized (SPC) process was then carried out at 600ºC for 24 hours in N_2 ambient. After SPC crystallization, the photoresist (PR) was coated on the top of poly-Si thin film and then patterned into SDA structure through laser interference lithography as shown in the Figure 1a. The scanning electron microscope (SEM) image and atomic force microscope (AFM) image of SDA patterns after lithography are shown in Figure 2a and Figure 2b respectively. The diameter (d) of submicron dot is 0.5μm. Boron ions were then implanted into the exposed areas of the SPC ploy-Si film, as shown in the Figure 1a. After implantation, the PR was removed and the SDA doping pattern is formed as shown in Figure 1b. Then active islands were patterned, followed by 100nm low temperature oxide (LTO) deposition as gate dielectric. Then 300nm aluminum was sputtered and patterned as gate electrode. Next, self-aligned 35keV boron implantation was done at a dosage of 4×10^{15}cm^{-2}. 500nm LTO was then deposited and contact holes were defined. 700 nm Al-1%Si was sputtered. After patterning the metal layer, the devices were sintered in forming gas for 30 min at 420ºC. No further passivation was applied to these devices. The cross-sectional of device structure is shown in Figure 1c. The fabricated TFT with SDA doped channel is named SDA TFT. For the control wafer, no SDA doping is performed.

For characterizations, the Agilent 4156C semiconductor parameter analyzer is used to test the devices' transfer and output curves. The μ_{FE} is extracted from expression,

$$\mu_{FE}=\frac{Ld_{ox}G_m}{W\varepsilon_{ox}V_{ds}}$$

where d_{ox}, ε_{ox} and G_m are physical gate dielectric thickness, gate dielectric permittivity and maximum of transconductance at V_{ds}=−5V.The *SS* is defined by the slope of log|I_d| in 10^{-10}A range at V_{ds}=−5V. The I_{on}/I_{off} ratio equals to maximum current over minimum current within the measure range at V_{ds}=−5V. All TFTs used in this study have width (W) / length (L) =10/10 μm.

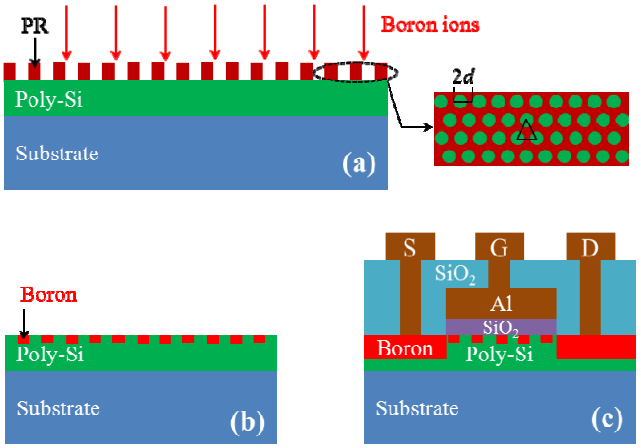

Figure 1: (a) The cross-sectional schematic and top view of SDA pattern formation. (b) The cross-sectional schematic of active channel with SDA boron doping. (c) The cross-sectional of device structure.

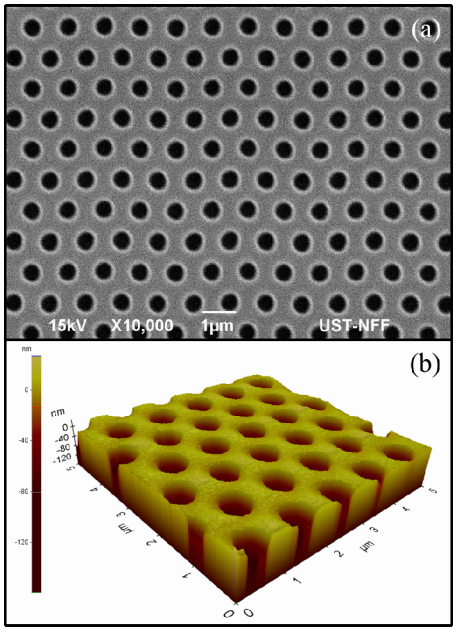

Figure 2: (a) SEM image and (b) AFM image of SDA pattern after lithography.

3. Results and Discussion

The transfer characteristics of SDA TFT and control TFT are shown in Figure 3. The inset are transfer curves plotted in the linear scale, measured at V_{ds}=−0.1V. Compared to the control TFT, SDA TFT obviously show better performance in terms of higher I_{on}, steeper *SS* and lower gate-induced drain leakage (*GIDL*) current [8]. The μ_{FE} increases to 58.4cm^2/Vs for SDA TFT with d=0.5μm, which is 4 times of control TFT without SDA doping. The measured data and the extracted device parameters are summarized in Table I.

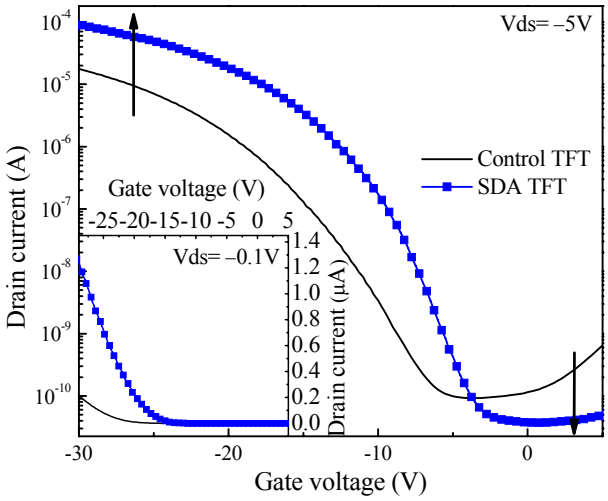

Figure 3: Transfer curves of SDA TFT and control TFT plotted in logarithmic scale, measured at V_{ds}=−5V. The inset are transfer curves in the linear scale, measured at V_{ds}=−0.1V.

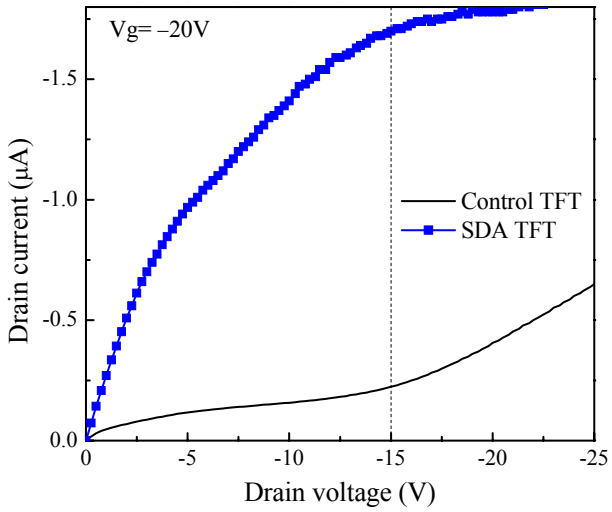

Figure 4: Output curves of SDA TFT and control TFT measured at V_g=−20V.

Table I
Device parameters of SDA TFTs and control TFTs

	μ_{FE} (cm^2/Vs)	*SS* (*V/dec*)	I_{on}/I_{off} ($\times 10^5$)
Control TFTs	14.6	1.49	5.09
SDA TFTs	58.4	1.02	51.94

Shown in the Figure 4 are output curves of SDA TFT and control TFT measured at Vg=−20V. Consistent with transfer curves shown in Fig.4, SDA TFT exhibits lager on current. Besides enhancing on current, it can be also observed that the kink current can be greatly suppressed by employing SDA structures, indicating improved hot carrier reliability [7-8].

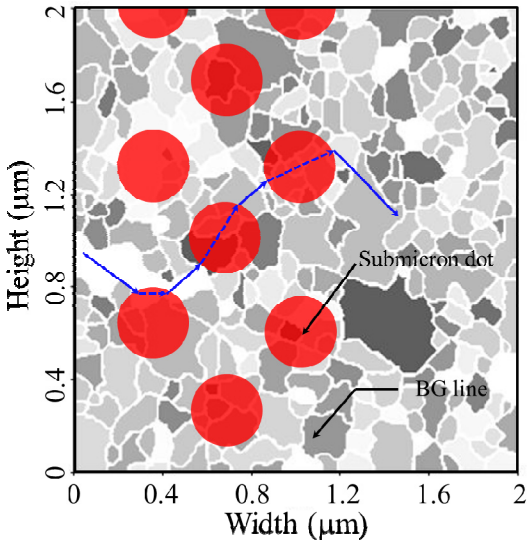

Figure 5: Schematic of current flow in poly-Si thin film with SDA doping based on grain detection result.

To understand the conduction mechanism of SDA TFTs, the SPC poly-Si film is first treated by tetramethylammonium hydroxide etching. Then AFM is applied to confirm the grain size through examining the surface topography. With the help of the AFM watershed grain detection program [9], it was found that the mean value of the grain size is about 150nm, as shown in Figure 5. These small size grains result in high GB density. When the carries transfer from drain to source, they will surmount lots of barriers at GBs and thus limiting the on current. As discussed in ref. [7], when the carrier flows, it will pick the most direct path with less GBs. Once the carrier enters into doped region, it can pick any path freely since in the heavily doped region no barriers are supposed to be existed. In Figure 5, the red dots represent for heavily doped SDA. The principle of SDA is to build bridges to link the small grains and enhance on current, as indicated by blue arrows in Figure 5. For the off state, the *GIDL* current increases exponentially as a function of this reverse electric field [8]. The SDA structure can effectively terminate the electric field, resulting in lower GIDL current, compared to the control TFT.

4. Conclusion

In this work, the SPC poly-Si TFTs using SDA doped channel is first demonstrated. By employing SDA method, the device performance is greatly enhanced, especially for improvement of μ_{FF}. The conduction mechanism of SDA TFTs is analyzed and discussed.

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