High-Performance Polycrystalline Silicon Thin-Film Transistors Based on Metal-Induced Crystallization in an Oxidizing Atmosphere

Rongsheng Chen, Wei Zhou, Meng Zhang, Man Wong, *Senior Member, IEEE*, and Hoi-Sing Kwok, *Fellow, IEEE*

***Abstract*— An oxidizing rather than the commonly used nonoxidizing atmosphere is used to carry out the thermal process required by the metal-induced crystallization (MIC) of amorphous silicon. Thin-film transistors fabricated on the resulting polycrystalline silicon (poly-Si) exhibit improved device characteristics. Since thermal oxidation is known to induce the injection of silicon interstitials, the improvement is attributed to a reduction in the defect population caused by the incorporation of the injected silicon interstitials in the grain boundaries of the MIC poly-Si.**

***Index Terms*— Polycrystalline silicon, thin-film transistors (TFTs), metal-induced crystallization (MIC), oxygen annealing.**

I. Introduction

POLYCRYSTALLINE silicon (poly-Si) thin-film transistors (TFTs) are excellent candidates for the next generation flat-panel displays, particularly those based on organic light-emitting diodes. The higher mobility of poly-Si TFTs than that of amorphous silicon (a-Si) TFTs allows higher aperture ratio when used as switching and driving transistors in the pixels and offers the possibility of integrating peripheral circuits with the pixel matrix, thus realizing a system on panel [1].

Much effort has been made to improve the quality of the poly-Si, since it is one of the key factors that determine the performance of a TFT. The three most popular crystallization methods are solid-phase crystallization (SPC) [2], metal-induced crystallization (MIC) [3] and excimer laser crystallization (ELC) [4]. The SPC process is the simplest method to obtain a poly-Si thin film. However, the electrical performance of the resulting TFT is poor. ELC employs laser as a local heating technique to induce the crystallization, producing the best quality film. The drawback of ELC is the high cost of the equipment, inferior uniformity and lower process throughput. Compared to SPC, MIC has the advantage of a shorter process time, lower process temperature and higher carrier mobility; compared to ELC, MIC offers better uniformity and lower cost.

Manuscript received November 25, 2014; revised December 19, 2014, January 5, 2015, and February 3, 2015; accepted February 27, 2015. Date of publication March 9, 2015; date of current version April 22, 2015. This work was supported by the Research Grants Council, Hong Kong Government within the Theme-Based Research Scheme under Grant T23-713/11-1. The review of this letter was arranged by Editor W. S. Wong.

The authors are with the State Key Laboratory on Advanced Displays and Optoelectronics Technologies, The Hong Kong University of Science and Technology, Hong Kong (e-mail: rschen@connect.ust.hk).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2015.2409858

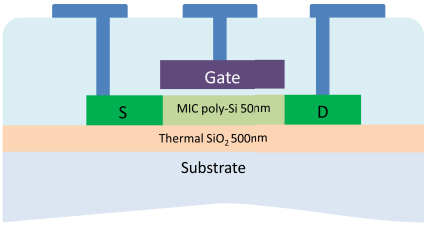

Fig. 1. Cross-sectional schematic of the poly-Si TFTs with self-aligned structure.

The atmosphere used in the SPC and MIC annealing process are traditionally non-oxidizing, typically nitrogen [5], [6]. A. Yin *et al.* proposed that oxygen plasma exposure for a-Si film can produce a super saturation of silicon atoms below the Si/SiO_2 interface and enhance poly-Si grain growth during SPC in furnace or rapid thermal annealing [7]. T. Kamiya *et al.* reported that hot H_2O-vapor annealing could effectively reduce the grain-boundary dangling bonds, lower the potential barrier height and narrow the distribution of the barrier height value [8]. These reports demonstrated that annealing or treatment in an oxidizing atmosphere could help improve the quality of SPC poly-Si thin film. However, these methods require additional steps and increase the process complexity and manufacture cost. Furthermore, to our knowledge, there is no report on the MIC of a-Si in an oxidizing atmosphere.

In this letter, a simple method to improve the material quality of poly-Si thin film formed using MIC is developed. The annealing process required by MIC is carried out in an oxidizing atmosphere rather than the traditional non-oxidizing atmosphere. The defect density of poly-Si thin film is reduced due to the incorporation of silicon interstitials generated and injected in the grain boundaries during the modified MIC process. TFTs fabricated on the resulting poly-Si thin film exhibit improved device performance, including higher field-effect mobility and lower threshold voltage.

II. Experimental

The cross-sectional schematic of the proposed MIC poly-Si TFTs is shown in Figure 1.

TABLE I
ANNEALING CONDITION FOR SAMPLES A, B, C, D, AND E

Sample	Stage 1 N_2 annealing (hrs)	Stage 2 O_2 annealing (hrs)	Total Annealing Time (hrs)
A (Control)	10	0	10
B	0	10	10
C	2	8	10
D	1	9	10
E	0.5	9.5	10

The fabrication process began with 4-inch silicon wafers covered with 500-nm thick thermal oxide. 45-nm thick a-Si was deposited as active layer by low-pressure chemical vapor deposition (LPCVD). A thin layer of nickel was deposited on top of the a-Si layer. The MIC process was then carried out by annealing at 600 °C for fixed total annealing time of 10 hours in a furnace under different conditions, as summarized in Table I. 10-hours N_2 annealing is considered sufficient for MIC process. In our experiment, we introduced an oxidizing atmosphere without increasing the thermal budget. O_2 is used as the reactive gas. It is worth mentioning that other oxidizing gases, such as H_2O and N_2O, are also possible candidates which may work in a similar way. After the crystallization, the unreacted nickel was removed using a mixture of hot H_2SO_4 and H_2O_2. Any SiO_2 formed during the annealing or nickel cleaning process was removed through HF dipping.

The MIC poly-Si layer was then patterned to form the active islands. 50-nm thick SiO_2 was deposited by LPCVD at 425 °C as the gate dielectric. 300-nm thick Al was then deposited by sputtering and patterned as gate electrode. Self-aligned source and drain regions were implanted with boron at dose of 4×10^{15} /cm^2 and an energy of 20 keV. 500-nm thick SiO_2 was deposited by LPCVD as the passivation layer before the contact holes were defined. 700-nm thick Al-1% Si was sputtered and patterned as the metal leads. Finally, the devices were sintered in forming gas for 30 min at 420 °C. The electrical properties of the MIC poly-Si TFTs were measured at room temperature using an HP 4156B semiconductor parameter analyzer. The respective channel length (L) and width (W) of the devices are 10 and 10 μm.

III. RESULTS AND DISCUSSION

The typical transfer characteristics of MIC TFTs based on these poly-Si Samples are shown in Figure 2(a). The output characteristics of TFTs based on Sample A (1-stage N_2 annealing) and B (1-stage O_2 annealing) are shown in Fig. 2(b). Compared to the Sample A, the Sample B exhibits larger on-state current and lower threshold voltage. The distributions of the field-effect mobility and threshold voltage (V_{th}) for the Samples A, B, C, D, and E are shown in Figure 3. Twenty devices are measured for each sample. The extracted field-effect mobility of the Sample B is increased by 28%. The improvement of the TFT performance for the Sample B is

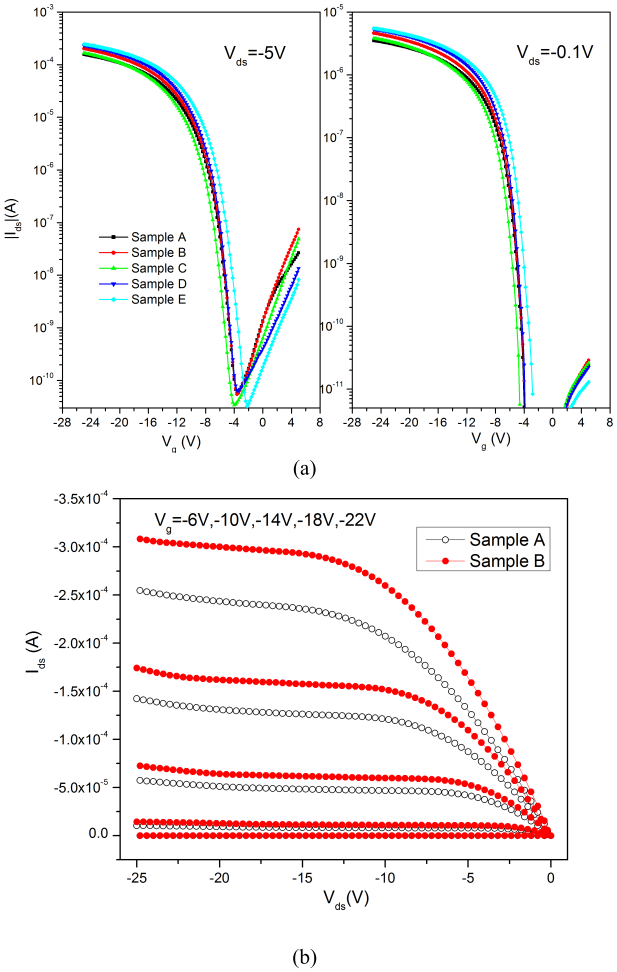

Fig. 2. (a) Transfer and (b) output characteristics of the poly-Si MIC TFTs.

attributed to the oxidizing annealing process, during which a thin SiO_2 layer is thermally grown on the surface of the poly-Si layer and silicon interstitials are generated and injected [9]. When the surface of silicon is oxidized, a volume expansion occurs and induces stress. Part of the stress can be relieved by injecting silicon interstitials into the bulk. This effect also causes enhanced diffusion and has been well studied [10]. Oxidation at high temperature (above 1000 °C) results in fast diffusion of oxygen and enables high generation rate of silicon interstitials. D. Skarlatos *et al.* has estimated the number of interstitials injected in silicon during thin oxide formation at a relatively low temperature through measurement of the end of range (EOR) defects [11]. It is shown that a 600 min 850 °C oxidation results in 6×10^{14} /cm^2 silicon atoms injected into silicon bulk. However, up to now it is still difficult to accurately estimate the generation rate of silicon interstitials at a temperature below 700 °C. In our case, the temperature is 250 °C lower than that reported by D. Skarlatos *et al.* while the duration is 10 hours. The thickness of oxide is measured to be about 2-3 nm and the amount of silicon interstitials injected into silicon bulk is estimated to be at the level of 10^{13} /cm^2.

In our experiment, the thin thermal oxide layer formed during oxygen annealing is removed before active

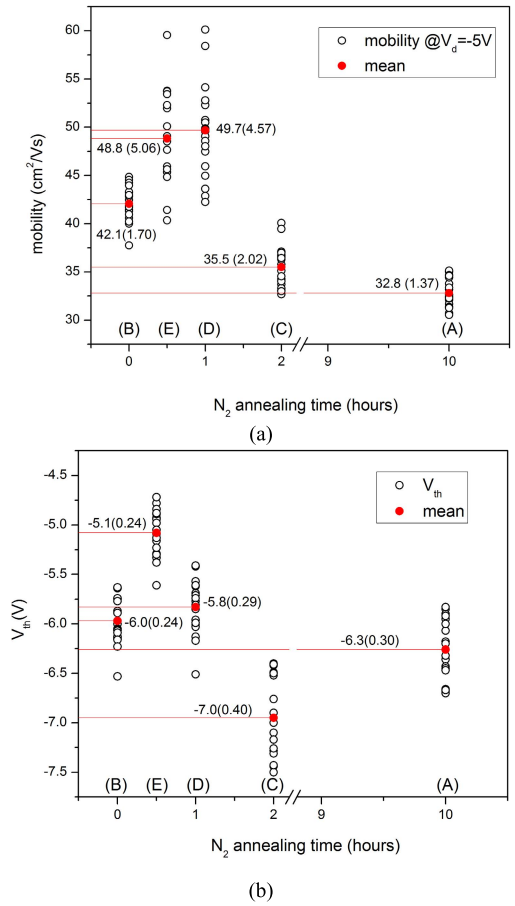

Fig. 3. The distributions of (a) field-effect mobility and (b) threshold voltage for sample A, B, C, D, and E. The mean and standard deviation (in the brackets) are labeled on the figures.

layer patterning. Therefore, the effect of possible gate dielectric interface change is eliminated. The improvement of TFT characteristics is attributed to the injection of Si interstitials. These interstitials diffuse into the film and are incorporated in the grain boundaries, which reduce the defect density of the MIC poly-Si thin film. The potential problem with the process for the Sample B is that the nickel catalyst was in direct contact with oxygen at the beginning of the annealing process. It has been reported that Ni diffusion and its reaction with Si may be degraded when MIC was carried out in an oxidizing atmosphere [12]. To optimize the MIC process, the annealing process was split into two stages for the Samples C, D, and E. In the first stage, the crystallization was initiated in nitrogen. The nickel catalyst was driven into the a-Si film without being oxidized. After this drive-in process, the atmosphere was switched to an oxidizing one to complete the crystallization (stage 2). The thin native SiO_2 formation and generation and diffusion of silicon interstitials were realized in the second stage.

From Figure 3 (a), the mobility of the Samples D and E do not show much difference, it indicates that 0.5 hour is enough for the drive-in process. The mobility of the Sample C is lower than that of sample D and E, reflecting that 8 hours of crystallization in an oxidizing atmosphere has resulted in the generation of an amount of silicon interstitials that is less than sufficient.

With the optimal two-stage annealing MIC process, the Samples D and E exhibit much better electrical performance. As compared with the Sample A, the field-effect mobility is 1increased by 51%. Moreover, the Sample E demonstrated the lowest threshold voltage. It has been reported that the threshold voltage is strongly influenced by the density of dangling bond associated with the mid-gap states and the field-effect mobility is related to the strain-bond tail states [13]. The lower threshold voltage of the Sample E may reflect a further reduction of dangling bond mid-gap states than the Sample D.

IV. Conclusion

A method to improve the material quality of poly-Si thin film formed using MIC is developed. The annealing process required by the MIC is split into two stages. The nickel catalyst is driven into the a-Si film in a nitrogen atmosphere during the first stage. The thin native thermal SiO_2 formation and generation of silicon interstitials were realized in an oxygen atmosphere during the second stage. The defect density of the poly-Si film is reduced due to the diffusion of silicon interstitials to the grain boundaries. Thin-film transistors fabricated on the resulting poly-Si thin film exhibit much improved device performance.

References

[1] Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 404–409, Feb. 2000.

[2] N. Yamauchi and R. Reif, "Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization: Theory, experiments, and thin-film transistor applications," *J. Appl. Phys.*, vol. 75, no. 7, pp. 3235–3257, Apr. 1994.

[3] S. Y. Yoon *et al.*, "Structural and electrical properties of polycrystalline silicon produced by low-temperature Ni silicide mediated crystallization of the amorphous phase," *J. Appl. Phys.*, vol. 87, no. 1, pp. 609–611, Jan. 2000.

[4] T. Sameshima, S. Usui, and M. Sekiya, "XeCl excimer laser annealing used in the fabrication of poly-Si TFT's," *IEEE Electron Device Lett.*, vol. 7, no. 5, pp. 276–278, May 1986.

[5] W. Zhou *et al.*, "Bridged-grain solid-phase-crystallized polycrystalline-silicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1414–1416, Oct. 2012.

[6] M. Wang, Z. Meng, and M. Wong, "The effects of high temperature annealing on metal-induced laterally crystallized polycrystalline silicon," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2061–2067, Feb. 2000.

[7] A. Yin and S. J. Fonash, "Oxygen-plasma-enhanced crystallization of *a*-Si:H films on glass," *J. Vac. Sci. Technol. A*, vol. 12, no. 4, pp. 1237–1240, Jul./Aug. 1994.

[8] T. Kamiya *et al.*, "Reduction of grain-boundary potential barrier height in polycrystalline silicon with hot H_2O-vapor annealing probed using point-contact devices," *J. Vac. Sci. Technol. B*, vol. 21, no. 3, pp. 1000–1003, May/Jun. 2003.

[9] R. E. Proano and D. G. Ast, "Effects of the presence/absence of HCl during gate oxidation on the electrical and structural properties of polycrystalline silicon thin-film transistors," *J. App. Phys.*, vol. 66, no. 5, pp. 2189–2199, Sep. 1989.

[10] S. M. Hu, "Formation of stacking faults and enhanced diffusion in the oxidation of silicon," *J. Appl. Phys.*, vol. 45, no. 4, pp. 1567–1573, 1974.

[11] D. Skarlatos *et al.*, "Estimation of the number of interstitial atoms injected in silicon during thin oxide formation," *J. Electrochem. Soc.*, vol. 146, no. 6, pp. 2276–2283, 1999.

[12] Z. Jin *et al.*, "Nickel induced crystallization of amorphous silicon thin films," *J. Appl. Phys.*, vol. 84, no. 1, pp. 194–200, Jul. 1998.

[13] I.-W. Wu *et al.*, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Lett.*, vol. 12, no. 4, pp. 181–183, Apr. 1991.