Substrate Current and Its Correlation with Degradation of Poly-Si Thin Film Transistors

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***Abstract*- Substrate current (I_{sub}) in poly-Si thin film transistors (TFTs) is first investigated by considering their specific substrate contact configuration. When the substrate bias is very small, I_{sub} is driven by the recombination process in the channel region and is related to the trap density (D_t) wherein. Controlled by the gate bias (V_g), the recombination region varies from the whole channel area to a localized region near the drain, source or substrate terminal. Based on such observation, I_{sub} is used to monitor the hot carrier degradation in TFTs. The I_{sub}-V_g curve is applied to sensitively reflect the location of the hot carrier-induced damage region and evaluate the local D_t increase wherein.**

I. Introduction

Low temperature poly-Si thin-film transistor (poly-Si TFT) is a promising candidate for active-matrix displays with integrated peripheral circuits on the same glass panel [1]. It is important to characterize the poly-Si TFT itself as well as its degradation. Although the substrate current (I_{sub}) in MOSFETs is commonly employed to monitor the lateral electric field which directly causes the crucial hot carrier (HC) degradation [2], the application of I_{sub} in poly-Si TFTs was rarely proposed [3]. Until now, neither the mechanism of I_{sub} nor its correlation with the degradation has been clarified. In this paper, by considering specific substrate contact configuration in poly-Si TFTs, I_{sub} as a function of the gate bias (V_g) and substrate bias (V_{sub}) is investigated. At small V_{sub}, I_{sub} is driven by the recombination process and therefore corresponds to the trap density (D_t). Besides, controlled by V_g, the recombination area locates at the whole channel or its some parts. Finally, the I_{sub}-V_g characteristic is applied to accurately locate the HC damage region and sensitively detect the D_t increase wherein, which is consistent with the proposed mechanism of the HC effect.

II. Results and Discussions

A. Substrate Current in poly-Si TFTs

Shown in Fig.1 are planar (a) and cross-sectional (b) views of an n channel poly-Si TFT with W/L=25/10μm and W_{sub}/L_{sub}=1.6/6μm. Poly-Si channel layer was formed by solution-based metal-induced crystallization [4] of a-Si at 630˚C. The flat band voltage (V_{fb}) and the threshold voltage (V_{th}) are 0 and 10V, respectively.

First, the substrate contact structure is examined. As shown in Fig.1a, different from that of MOSFETs, in poly-Si TFTs substrate terminal is a p^+-diffused side contact to the floating poly-Si channel. When I_{sub} is measured, the source and drain are grounded while the substrate and gate terminals are biased. At the moment, carriers transport between the p^+ substrate contact and the n^+-diffused source or drain, through an intrinsic poly-Si body. Thus I_{sub} is a diode current of a lateral PIN structure [4], with the source and drain as two parallel n-terminals and the substrate contact as the p-terminal. To be more precise, I_{sub} is the current of a gated PIN diode [5], since the intrinsic poly-Si channel is controlled by the gate, as shown in Fig.1b. Apparently, I_{sub} consists of two current components $I_{sub,d}$ and $I_{sub,s}$ from the drain and source, respectively.

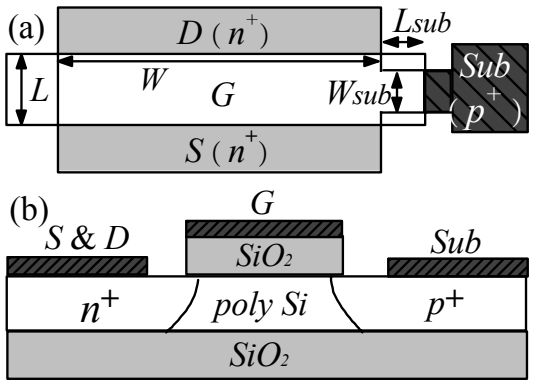

Fig. 1. Plane (a) and cross-sectional (b) views of poly-Si TFTs.

In a PIN structure, the difference in Fermi level (E_f) between the p^+ and n^+ terminals forms a potential barrier in the intrinsic region. At the p^+ substrate terminal, a positive V_{sub} reduces the potential and therefore I_{sub} is a forward current of the PIN diode which includes both diffusion and recombination currents [6-7]. As shown in Fig.2, I_{sub} as a function of V_{sub} are plotted in both linear and logarithmic scales. Not surprisingly, the I_{sub}-V_{sub} curve is very similar to the typical forward current of a normal PIN diode [8-9].

As shown in Fig.2, the I_{sub}-V_{sub} curve follows a well-defined exponential characteristic described by [4, 10]

$$I_{sub} = I_s \exp(qV_{sub}/mkT) \quad (1)$$

in which I_s, q, m, k and T are the saturation current, the electron charge, the ideality factor, the Boltzman constant and temperature, respectively. When V_{sub} is high (e.g., 2V), the potential barrier in the channel region is significantly reduced and thus most carriers can diffuse into the doped regions [6-7]. Therefore, I_{sub} is dominated by the diffusion current and in accordance with the channel carrier density. In contrast, if V_{sub} is very small (e.g., 0.07V), the barrier is not significantly lowered and most carriers are recombined in the channel region before

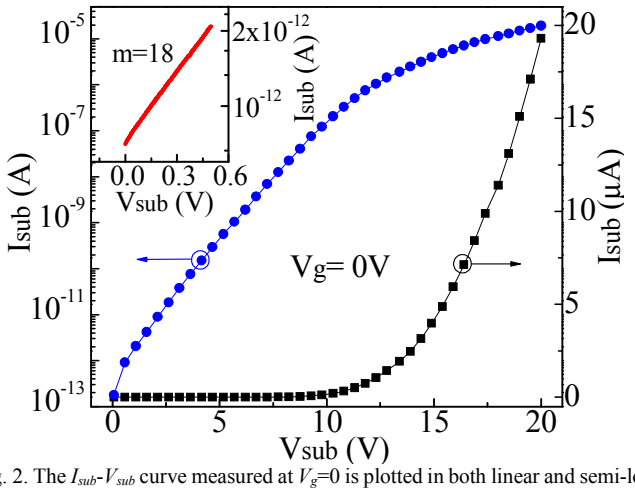

Fig. 2. The I_{sub}-V_{sub} curve measured at V_g=0 is plotted in both linear and semi-log scales. Besides, the curve in small V_{sub} range is replotted in semi-log scale, as shown in the inset.

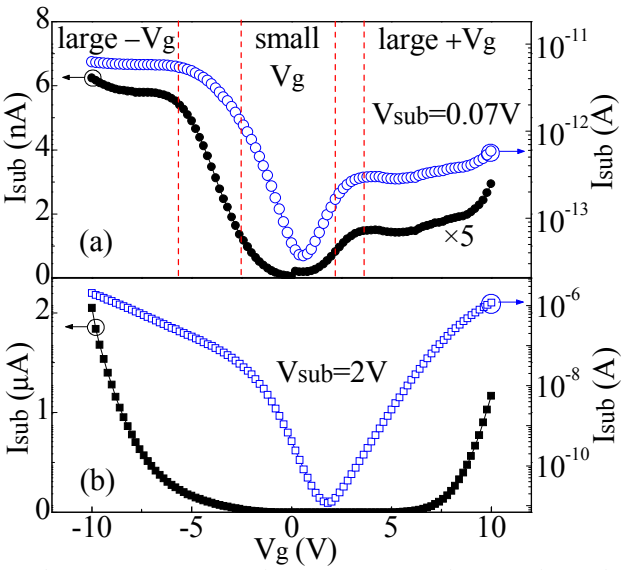

Fig. 3. The I_{sub}-V_g curves measured at V_{sub}=0.07V (a) and V_{sub}=2V (b) are plotted in both linear and semi-log scales. Besides, when V_g>0, I_{sub} at V_{sub}=0.07V is magnified by five times in the linear scale.

they can diffuse into the doped electrodes [6-7]. Thus, I_{sub} is controlled by the recombination process in the intrinsic region. As shown in the inset of Fig.2, the extracted m is far large than 2, which also strengthens the recombination nature of the current [4, 10].

In Fig.3a and 3b, I_{sub}-V_g curves are plotted in linear and semi-log scales, measured at V_{sub} = 0.07 and 2V, respectively. In small V_g range, both curves have a similar minimum I_{sub} around V_g=V_{fb} and I_{sub} increases exponentially with V_g. In large ±V_g range, I_{sub} at V_{sub}=0.07V gradually saturates and increases slowly, while I_{sub} at V_{sub}=2V does not saturate and still increases sharply. This discrepancy is due to the aforementioned different origins of I_{sub} depending on V_{sub}.

On the one hand, I_{sub} at V_{sub}=2V is a diffusion current and in proportional to the channel carrier density, which exponentially depends on V_g. Thus, I_{sub} also increases exponentially with V_g as shown in Fig.2b. While I_{sub} at V_{sub}=0.07V is a recombination current. Taking the -V_g range for example, the recombination current can be estimated by [4, 10]

$$I_{sub} \propto D_t A_r p \exp(qV_{sub}/mkT) \quad (2)$$

in which D_t, A_r and p are respectively the trap state density, area of the recombination region, and the channel hole density. As shown in Fig.4, the I_{sub}-V_{sub} curves at different V_gs agree well with Eq.2. Besides, m»2 further confirms the recombination mechanism [4, 10]. In Eq.2, not only p increases exponentially with V_g, but also A_r greatly depends on V_g. In other words, V_g controls I_{sub} mainly by affecting p and A_r.

As for A_r, the circumstance is complicated. In the small -V_g range, the channel is nearly intrinsic and the potential between the p^+ and n^+ terminals drops all along the channel. Therefore, A_r is always the whole channel region as shown in Fig.5a. Thus, in small -V_g range, I_{sub} exponentially increases with V_g. In the large -V_g range, the channel is in p-type and forms conductive path connecting the p^+ substrate. Thus PN junctions are formed near the drain and source, as indicated as D and S junctions in Fig.5b. In this case, A_r becomes the area of the two junctions. Therefore, in large -V_g range, although p still increases with V_g, A_r dramatically decreases from the whole channel region to the two junction regions. This explains why I_{sub} with V_{sub}=0.07V first

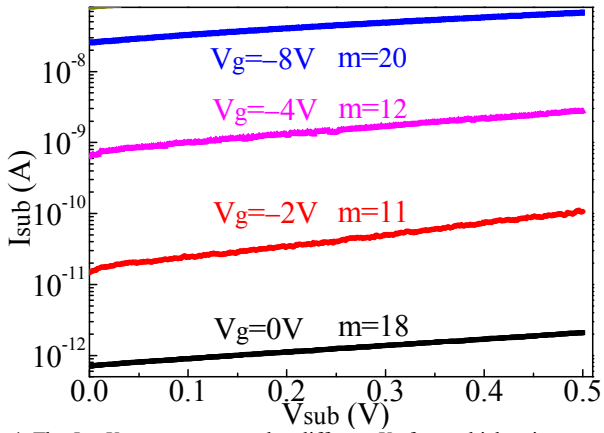

Fig. 4. The I_{sub}-V_b curves measured at different V_g, from which m is extracted.

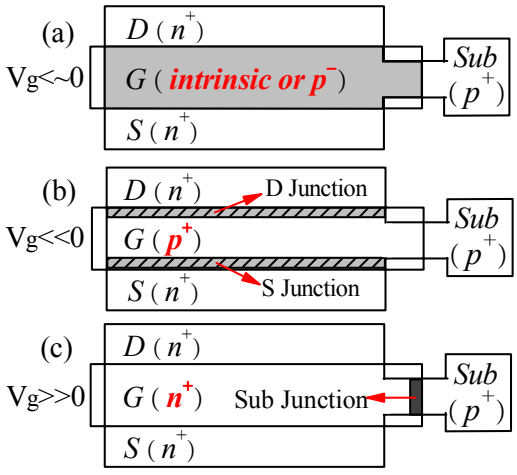

Fig. 5. The schematic diagrams of the plane views of poly-Si TFTs under various V_g circumstances: (a) V_g<~0; (b) V_g<<0; (c) V_g>>0. The shadow regions indicate the recombination areas for I_{sub} measured at small V_{sub}.

exponentially increases with V_g but becomes saturated or even drops a little as V_g increases further, as shown in Fig.3a. In the $+V_g$ range, similar mechanism occurs, except that under the high $+V_g$, A_r shrinks more dramatically, i.e., from the whole channel region to the small "sub-junction" area, as indicated in Fig.5c.

As for the I_{sub}-V_g curve at V_{sub}=0.07V, it has not gone unnoticed that I_{sub} in the $+V_g$ range saturates at a much smaller level than that for $-V_g$ range, which also derives from the V_g dependence of A_r. A_r at large $+V_{sub}$ is the area of the Sub junction, while A_r at large $+V_{sub}$ is the area of the D and S junctions, as shown in Fig.5. The former is much smaller than the later, because the width of the Sub junction (i.e., W_{sub}) is dramatically smaller than that of the D or S junction (i.e., W), as shown in Fig.1a. Therefore, according to Eq.2, I_{sub} in the large $-V_g$ range is notably smaller that that of large $+V_g$, as shown in Fig.3a.

B. Correlation between I_{sub} and HC Degradation

Shown in Fig.6 is the time evolution of the transfer characteristic under a typical HC stress with V_g=12V and V_d=20V [11]. Not surprisingly, the transfer curve typically degrades with V_{th} increasing and ON-current (I_{on}) decreasing (as indicated by the red arrow), while the subthreshold region is little affected. This is ascribed to that energetic HCs are generated by the high electric field near the drain during HC stress, and cause damage (or D_t increase) to grain boundaries (GBs) and/or Si-SiO_2 interface therein [11].

I_{sub}-V_{sub} curves at V_{sub} of both 2V and 0.07V are measured during HC degradation. However, the I_{sub}-V_g curve at V_{sub}=2V almost does not change under HC stress, As shown in the Fig.6 inset. It is because that such I_{sub} is a diffusion current and is not sensitive to D_t variation. In contrast, the I_{sub}-V_g curve at V_{sub}=0.07V does change with HC stressing, as shown in Fig.7. I_{sub} at V_{sub}=0.07V is a recombination current and in proportional to D_t according to Eq.2. More Detailedly, I_{sub} in the small V_g range only changes a little, indicating that D_t in the whole channel region does not vary much. In the high $+V_g$ range, I_{sub} is not visibly affected by the HC stress either, suggesting that D_t in the sub junction area does not change. While in high $-V_g$ range, I_{sub} continuously increases with stress time, suggesting that the

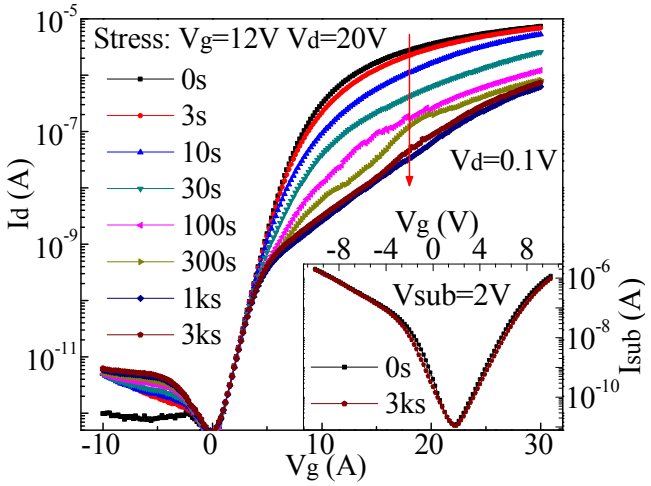

Fig. 6. The time evolutions of the transfer characteristic with V_g=0.1V and the I_{sub}-V_g curve with V_{sub}=2V under typical HC stress with V_g=12V, V_d=20V.

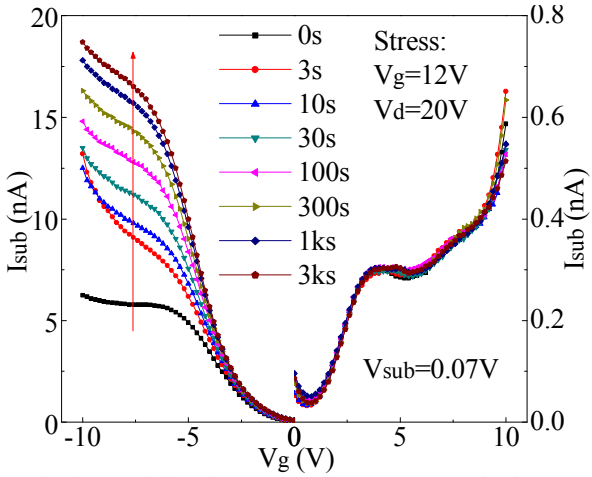

Fig. 7. The time evolution of I_{sub}-V_g curve at V_{sub}=0.07V under the HC stress with V_g=12V, V_d=20V.

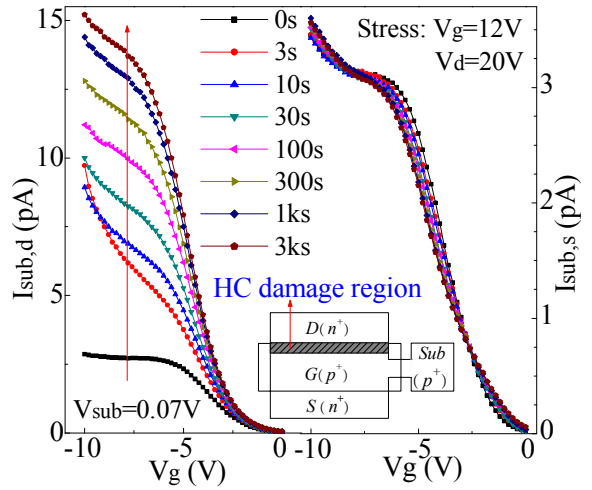

Fig. 8. The time evolutions of $I_{sub,d}$-V_g and $I_{sub,s}$-V_g curves with V_{sub}=0.07V under the HC stress with V_g=12V, V_d=20V. Besides, the HC damage region is shown in the inset.

D_t increases in the S junction and/or D junction. In order to further locate the region where D_t increases, the stress time evolutions of the two I_{sub} components, i.e., $I_{sub,d}$ and $I_{sub,s}$ are compared in Fig.8. It is interesting that $I_{sub,d}$ continuously increases in high $-V_g$ range while $I_{sub,d}$ almost keep unaffected. Therefore, I_{sub} increase totally originates from the $I_{sub,d}$ increase, which clearly indicates that D_t increase or the HC damage occurs only near the drain junction, as shown in the inset of Fig.8. This is well consistent with previous studies [11].

It would much desirable to evaluate the D_t increase in the HC damage region. The charge pumping (CP), as a generally accepted characterization method of D_t [12], has been successfully optimized in poly-Si TFTs and applied to reliably determine D_t [13]. Also, the CP has been employed to investigate the degradation of TFTs [14]. As shown in Fig.9, the CP current (I_{cp}) is little affected under the HC stress with V_g=12V and V_d=20V. The slight reduction of I_{cp} (ΔI_{cp}) indicates a small D_t decrease, which is undoubtedly in contradiction with the notable degradation of I_{on} (ΔI_{on}), as shown Fig.10. It suggests that the CP has difficulties in evaluating the HC

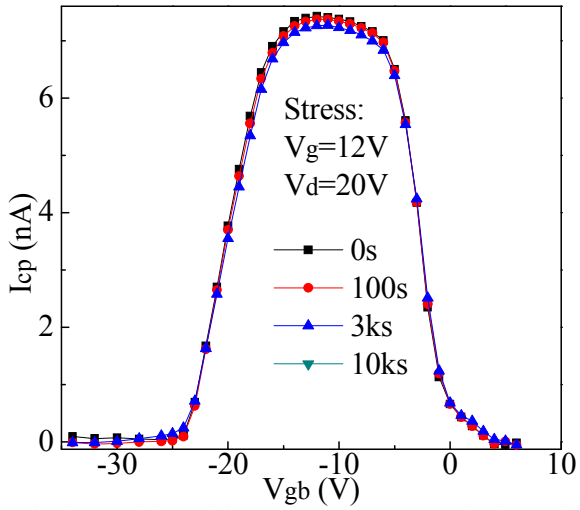

Fig. 9. The time evolutions of the CP curve, i.e., I_{cp} versus the base voltage of gate pulse (V_{gb}) under HC stress with V_g=12V, V_d=20V.

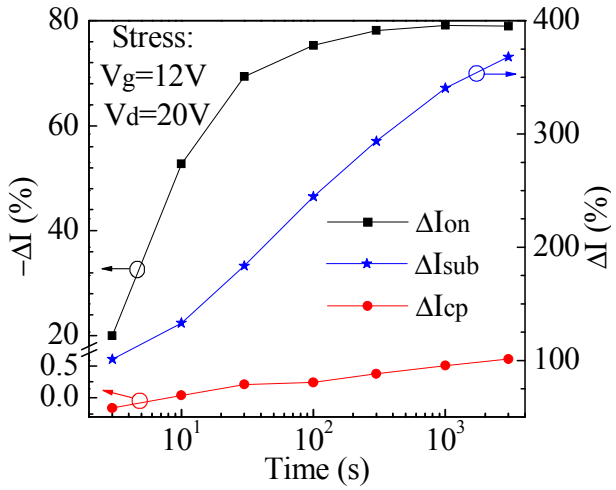

Fig.10. The time dependence of the ΔI_{cp} obtained from the CP curves of Fig.9 with V_{gb}=-12V, the ΔI_{sub} extracted from the $I_{sub,d}$-V_g curves of Fig.6 with V_g=-8V and ΔI_{on} determined from transfer curves in Fig.5 with V_g=15V.

degradation [14], because the CP is only sensitive to the D_t of the whole channel [12] while the HC-induced D_t increase occurs locally in the D junction.

On the contrary, such local D_t increase can be estimated from the time evolution of $I_{sub,d}$ with V_{sub}=0.07V in Fig.8. As mentioned above, in high -V_g range (e.g., -8V), $I_{sub,d}$ derives from the recombination process in the D junction and therefore is in accordance with the D_t in the HC damage region near the drain terminal, according to Eq.2. As shown Fig.10, the obvious increment of $I_{sub,d}$ with V_{sub}=0.07V and V_g=-8V reflects a notably D_t increase in the HC damage region, which will form a high barrier near the drain and therefore dramatically reduce I_{on} [11]. This is well consistent with the dramatic I_{on} degradation show in Fig.10.

III. Summary

The mechanism of I_{sub} in poly-Si TFTs is first clarified. I_{sub} is found to be a diode of a gated PIN Structure and I_{sub} at low V_{sub} is driven by the recombination process in the channel region. Besides, under the control of V_g, the recombination area locates at the whole channel or the local area near drain, source or substrate terminal. Based on this insight, the I_{sub}-V_g curve together with its two component, i.e., the $I_{sub,d}$-V_g and $I_{sub,s}$-V_g curves is applied to investigate the HC degradation of poly-Si TFTs. Not only is the HC damage region accurately located, but also the HC-induced D_t increase near the drain is sensitively detected, which easily overcomes the deficiency of the CP on the HC investigation.

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