Annealing-Induced Depletion-Mode Indium-Gallium-Zinc Oxide Thin-Film Transistor and Its Application to Active-Matrix Organic Light-Emitting Diode Display

Lei Lu*, Yi-Bin Jiang, Jia-Peng Li, Zhuo-Qun Feng, Man Wong, Hoi-Sing Kwok

Department of Electronic and Computer Engineering, the Hong Kong University of Science and Technology, Kowloon, Hong Kong

ABSTRACT

During the fabrication of an indium-gallium-zinc oxide (IGZO) thin film transistor (TFT), the thermal process was used to reduce the resistivity of IGZO. The annealing temperature was found to have great influence on the transistor characteristics. At an optimized heat-treatment temperature, the depletion-mode IGZO TFT was fabricated with steeper subthreshold slope, higher filed-effect mobility and acceptable turn-on voltage. And the relatively conductive IGZO could directly replace the indium tin oxide as the transparent electrode of the organic light-emitting diode (OLED), reducing the mask count of the backplane for the active-matrix OLED display.

INTRODUCTION

Thin film transistor (TFT) based on metal oxide (MO), especially, indium-gallium-zinc oxide (IGZO), is considered as a good candidate to fabricate large area backplane for active-matrix organic light-emitting diode (AMOLED) display, due to its high mobility, good uniformity and low off-state current [1]. Our previous study [2] suggested that the resistivity (ρ) of IGZO highly depended on the heat-treatment conditions, such as annealing ambience, temperature, duration and gas permeability of IGZO cover, while the thermal process was often inevitable during the fabrication of IGZO TFT.

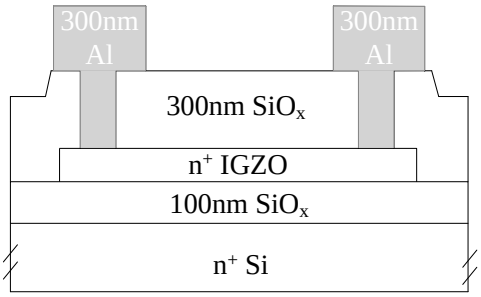
With the active layer of IGZO covered with the gas-permeable silicon oxide (SiO_x), the TFT was subjected to a serious anneals in an oxygen-deficient nitrogen (N_2) ambience. With the increasing temperature, although the mobility was enhanced, the turn-on voltage (V_{on}) became more and more negative. At an optimized temperature, the depletion-mode (DM) IGZO TFT with steeper subthreshold slope, higher filed-effect mobility and acceptable turn-on voltage was fabricated.

Furthermore, such annealing-induced conductive IGZO source/drain regions can be directly used to replace the indium tin oxide (ITO) as the transparent electrode of OLED, reducing the mask count of AMOLED backplane.

Annealing-Induced DM IGZO TFT

Shown in Figure 1 is the evolution of the schematic cross-section of an IGZO TFT. A gate dielectric of 100 nm silicon oxide (SiO_x) was first thermally grown on an n^+ silicon substrate, which served as the gate electrode. 10 or 20 nm IGZO film was then room-temperature sputtered using a target of In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol% in an atmosphere of 10% oxygen (O_2) and 90% argon (Ar). After the patterning of the active-island using the hydrofluoric acid, a passivation layer of 300 nm SiO_x was deposited at 300 ^oC in a plasma-enhanced chemical vapor deposition (PECVD) reactor. The tetraethylorthosilicate (TEOS) and O_2 were used as the source gases. The contact holes were then opened and the resulting structure was subjected to a series of anneals, as shown in Figure 1a. Finally, 300 nm aluminum (Al) was deposited and patterned into electrodes (Fig. 1b). These TFTs were measured using an Agilent 4156C semiconductor parameter analyzer.

(a) Thermal Annealing



(b) Electrodes

Figure 1. The schematic cross-section of an IGZO TFT during (a) thermal annealing and (b) electrode patterning.

The drain current (I_d) versus gate voltage (V_g)

transfer characteristics were measured at a drain voltage (V_d) of 5 V. Shown in Figure 2 were the transfer curves for TFTs subjected to 20-minute anneals in N_2 at various temperatures. Along with the increasing temperature, the TFT characteristics gradually evolved towards the negative V_g direction.

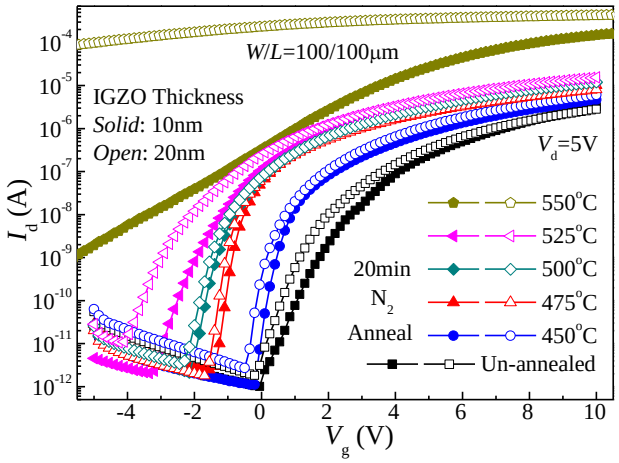


Figure 2. The transfer characteristics of IGZO TFTs subjected to a series of 20-minute isochronal anneals in N_2 at different temperatures.

To quantitatively analysis this evolution, the V_{on}, defined as the V_g corresponding to the minimum I_d, was plotted versus the annealing temperature in Figure 3. V_{on} gradually decreased with the increasing temperature and the TFT accordingly changed from the enhancement mode to the depletion mode. Such decrease of V_{on} was more serious for TFTs with thicker IGZO. At a high enough temperature (e.g., 550 °C), the transistor with 10 nm IGZO can no longer be effectively depleted, while that with 20 nm IGZO even behaved like a conductor, suggesting an annealing-induced conductive channel.

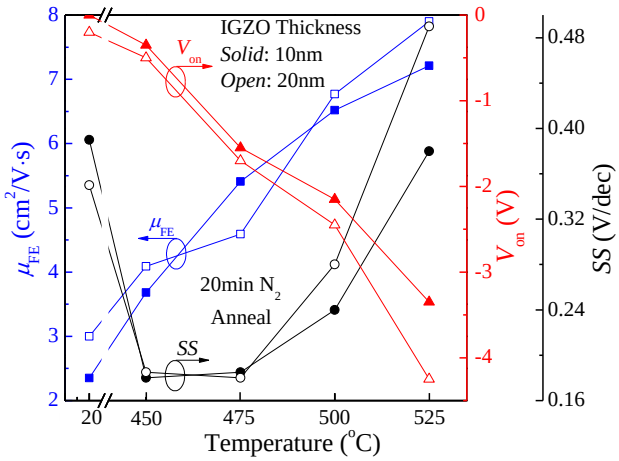


Figure 3. The temperature-dependence of μ_{FE}, V_{on} and SS for the annealed TFTs.

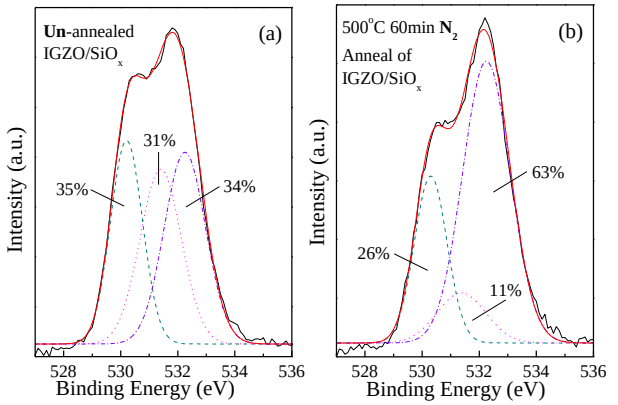


Figure 4. The XPS spectra of O 1s for IGZO/SiO_x sample (a) un-annealed or (b) subjected to 500 °C 60-minute anneal in N_2.

Since the passivation layer of SiO_x is gas-permeable, the oxygen species can thermally escape from IGZO to the N_2 ambience [2], generating donor-like defects and thus reducing IGZO ρ. The chemical state of O 1s in IGZO, known to be related to the defects and ρ, was then studied using the X-ray photoelectron spectroscopy (XPS) [3]. The IGZO covered with 100nm PECVD SiO_x was either un-annealed or subjected to 500°C 60-minute anneal in N_2. As shown in Figure. 4a, the O 1s peak can be resolved using Gaussian fitting into three sub-peaks, centered at 530.15 ± 0.15 eV, 531.25 ± 0.20 and 532.40 ± 0.15 eV, separately related to the stoichiometric oxygen, oxygen vacancy (V_o) defect and oxygen interstitial (O_i) defect, both known as donors [4]. For IGZO/SiO_x sample annealed in N_2, the area percentage of O_i peak dramatically increased from 34% to 63%, suggesting that the abundant generation shallow donor O_i is responsible for the annealing-induced conductivity.

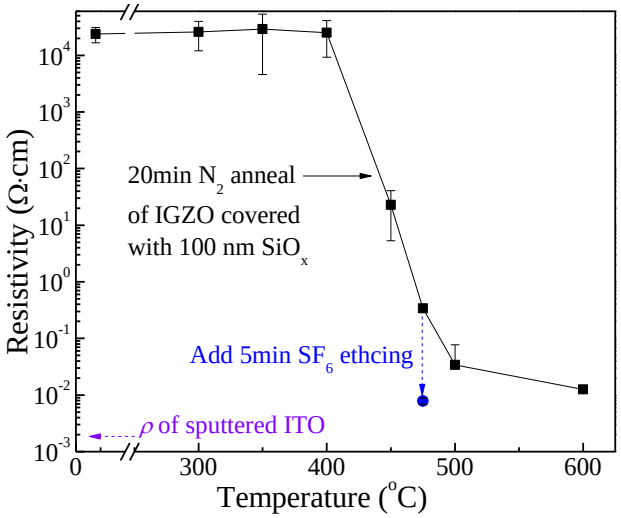


Figure 5. The temperature-dependence of the ρ of IGZO/SiO_x sample subjected to 20-minute anneals in N_2.

The thermal generation process of donor-like defects in IGZO highly depended on the heat-treatment temperature. As shown in Figure 5, the IGZO ρ decreased with the increasing temperature, in consistent with the temperature evolution of V_{on}. As shown in Figure 3, such annealing-induced oxygen-deficient IGZO channel also enhanced the file-effect mobility (μ_{FE}) [5], extracted using the maximum $\partial I_d^{0.5}/\partial V_g$ in the saturation regime of the TFT operation, and improved the subthreshold slope (SS) within a temperature range. The overall trade-off suggests 475 °C as an optimal anneal temperature, supplying higher μ_{FE}, steeper SS and acceptable V_{on}.

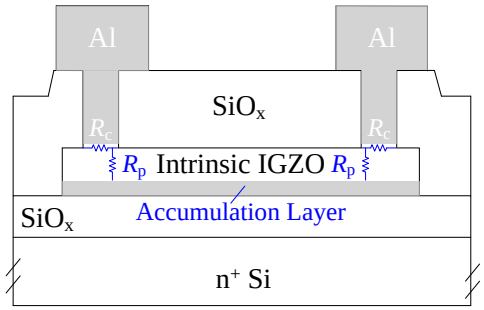


Figure 6. The schematic cross-section of an IGZO TFT, indicating the presence of R_p and R_c.

Such enhanced performance plausibly derives from that the annealing-induced donors suppress the barrier near the conduction band edge [6], which was known to obstruct the carrier transport in IGZO. Furthermore, the parasitic resistance (R_p) across the channel thickness [7] and the contact resistance (R_c) between IGZO and electrodes [8] (Fig. 6) can both be significantly decreased by increasing the IGZO conductivity. However, when the channel carrier concentration was raised too high, both SS and the off-state current tended to degrade, especially for TFTs with thicker IGZO, since more charges need to be depleted.

AMOLED Backplane Based on DM IGZO TFT

As shown in Figure 5, the ρ of annealed IGZO is higher than that of ITO but still low enough to serve as a transparent electrode of OLED, especially considering the short current path from TFT to OLED in a pixel circuit. Furthermore, the IGZO ρ could be even further reduced using a sulfur hexafluoride (SF_6) plasma etching (Fig. 5).

Shown in Figure 7a is the cross-sectional view of a five-mask backplane of AMOLED display based on the proposed DM IGZO TFT with the conductive n^+ IGZO to replace the common ITO as the transparent cathode of the OLED.

Furthermore, since most MO semiconductors are n-type, inverted structure of OLED with the bottom electrode as the cathode is preferred in order to facilitate the driving circuit design with n-channel MO TFTs. However, most transparent electrodes (e.g., ITO) have high work function (< –4.3 eV), which is lower than the lowest unoccupied molecular orbital (LUMO) level of most organic electron transportation materials (–3.3 eV ~ –2.7 eV). As a result, a large electron injection barrier from the bottom electrode to the electron transportation layer (ETL) exists.

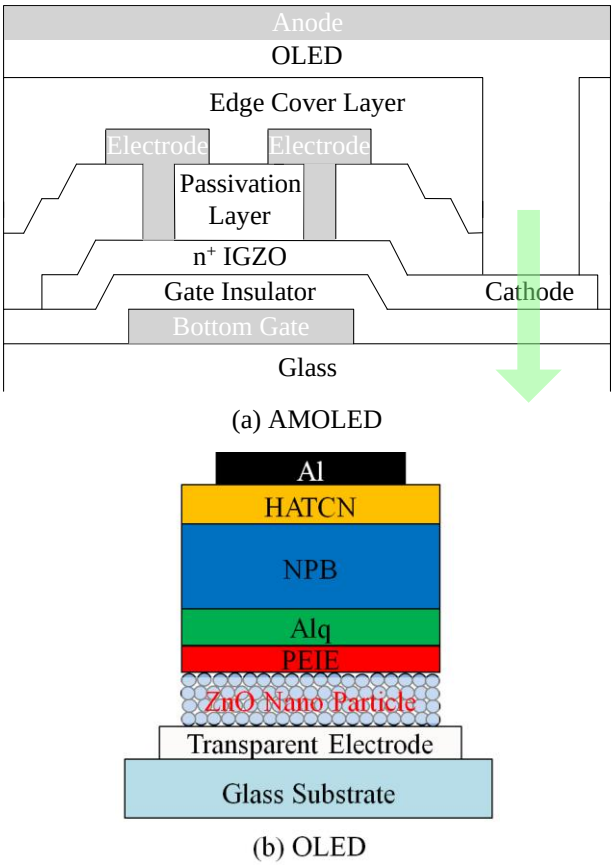


Figure 7. (a) The cross-sectional view of a five-mask backplane for AMOLED. (b) The layer structure of inverted OLED.

In this work, a hybrid inverted structure (Fig. 7b) was proposed for OLED with ZnO nanoparticles as ETL. The conduction band edge level of ZnO nanoparticles is around –4 eV, which is suitable for transparent electrodes (e.g, ITO or n^+ IGZO) to injection electrons into it. In order to help efficiently inject electrons from ZnO nanoparticles layer into organic layer, a very thin polyethylenimine ethoxylated (PEIE) layer was used to reduce the work function of ZnO from 4.2 eV to 3.2 eV [9]. With this inverted structure (S1), the electronic and optical performance of the device can be comparable to that of the conventional structure (S2) with the bottom electrode as the anode, as shown in Figure 8. The inverted device can be turned on at a low voltage of 2.6 V, and achieve a luminance of 1000 cd/m^2 at a driving voltage of 6V.

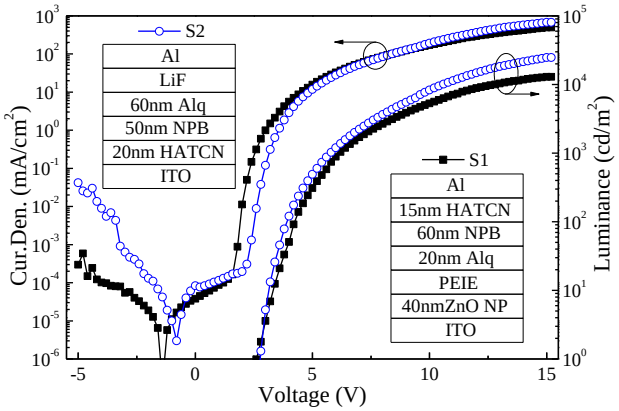


Figure 8. (a) Current density-voltage and (b) luminance-voltage characteristics of the proposed inverted OLED compared with those of conventional OLED.

Conclusions

During the fabrication of IGZO TFT, the oxygen-deficient anneal was used to reduce the IGZO ρ, since the oxygen can escape from IGZO though the gas-impermeable passivation layer of PECVD SiO_x, generating donor-like defects. The heat-treatment temperature was optimized to fabricate a DM IGZO TFT with enhanced performance and conductive IGZO source/drain regions. Such annealing-induced conductive IGZO could be directly used to replace ITO as the transparent electrode of OLED, reducing the mask count of the AMOLED backplane. An inverted OLED structure with the transparent electrode (e.g., ITO or conductive IGZO) as the cathode, which is preferred for the pixel circuit based on the n-channel MO TFT, was demonstrated and its performance was compatible with that of the traditional OLED.

Acknowledgements

This work was supported by Grant GHP/022/12SZ-2 from the Innovation and Technology Fund and Grant ITC-PSKL12EG02 from the Partner State Key Laboratory on Advanced Displays and Optoelectronics Technologies.

References

[1] J.S. Park, W.J. Maeng, H.S. Kim, and J.S. Park, *Thin Solid Films*, no. 520, p. 1679 (2012).

[2] L. Lu and M. Wong, *IEEE Trans. Electron Devices*, no. 62, p. 574 (2015).

[3] S. Bang, S. Lee, J. Park, W. Jeong, and H. Jeon, *J. Phys. D. Appl. Phys.*, vol. 42, no. 23, p. 235102 (2009).

[4] J. Robertson, *J. Non. Cryst. Solids*, vol. 358, no. 17, p. 2437 (2012).

[5] J.C. Park, S.-E. Ahn, and H.-N. Lee, *ACS Appl. Mater. Interfaces*, no. 5, p. 12262 (2013).

[6] T. Kamiya, K. Nomura, and H. Hosono, *J. Disp. Technol.*, no. 5, p. 462 (2009).

[7] R. I. Kondratyuk, K. Im, D. Stryakhilev, C. G. Choi, M.-G. Kim, H. Yang, H. Park, Y. G. Mo, H. D. Kim, and S. S. Kim, *IEEE Electron Device Lett.*, vol. 32, no. 4, p. 503 (2011).

[8] T.T. Trinh, K. Jang, S. Velumani, V.A. Dao, and J. Yi, *Mater. Sci. Semicond. Process.*, no. 38, p. 50 (2015).

[9] Y. Zhou, et. al., *Science*, no. 336, p. 327 (2012).